SULEYMAN DEMIREL UNIVERSITY
ENGINEERING FACULTY

DIGITAL DESIGN

TEST QUESTIONS with SOLUTIONS

COMPILER Mrs. L. Kiziyeva

Almaty
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1.Obtain the result of binary division: 11011101:00010001

A. 1101 B. 1010 C. 1001 D. 10101 E. 11101

True answer is: A. 1101

```
 11011101 | 10001
-10001    | 1101
  10101
 -10001
    10001
   -10001
        0
```

2. A basic operation in digital system is

A. Addition B. Multiplication C. Conversion D. Complementing

E. Inter-register transfer operation

True answer is: E. Inter-register transfer operation

3. The register's content is:

1	0	0	0	0	1	0	0	0	1	1	0

In BCD it represents:

A. 846 B.946 C. 856 D. 956 E. 945

True answer is: A. 846

1000 – 8 in BCD
0100 – 4 in BCD
0110 – 6 in BCD

4. The truth table for AND gate is:

A

x	y	F
0	0	0
0	1	0
1	0	0
1	1	1

B

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

C

x	Y	F
0	0	1
0	1	1
1	0	1
1	1	0

D

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

E

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

True answer is: A. Because AND gate true iff all inputs are true.

5. The truth table for XNOR gate is:

A

x	y	F
0	0	1
0	1	0
1	0	0
1	1	1

B

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

C

x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

D

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

E

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

True answer is: A. Because XNOR gate true if sum of inputs is even.

6. The content of register when we enter 249 in BCD is:

A	0	0	1	0	0	1	0	0	1	0	0	1
B	0	0	1	0	0	1	0	0	1	0	0	0
C	0	1	0	0	0	0	1	0	1	0	0	1
D	0	0	1	1	0	1	0	0	1	0	0	0
E	0	0	1	0	0	0	1	1	1	0	0	1

True answer is: A. 0010 0100 1001

7. Convert $(127.4)_8$ to decimal:
A.74.6 B. 67.5 C. 84.5 D. 87.6 E. 87.5
True answer is: E. 87.5 $1*8^2+2*8^1+7*8^0+4*8^{-1}=87.5$

8. Convert $(B65F)_{16}$ to decimal:
A. 35576 B. 46687 C. 35676 D. 46587 E. 45372
True answer is: B. 46687 $B(11)*16^3+6*16^2+5*16^1+F(15)*16^0=46687$

9. Convert $(010110001101011.111100000110)_2$ to octal:
A. 26153.7406 B. 27153.7406 C. 26351.7206 D. 26143.6406 E. 26153.7206
True answer is: A. 26153.7406 **010 110 001 101 011 . 111 100 000 110**
2 – 6 – 1 – 5 – 3 . 7 – 4 – 0 – 6

10. Convert $(0010110001101011)_2$ to hex:
A. 3B6C B. 3C6B C. 2C5B D. 2B6C E. 2C6B
True answer is: E. 2C6B **0010 1100 0110 1011**
2 - C(12) - 6 - B(11)

11. Convert $(673)_8$ to binary:
A. 110101011 B. 111110011 **C. 110111011** D. 110111100 E. 110111010
Answer: C
Solution:
To convert from radix r=8 to radix r=2 we should convert digit by digit as following: (since 8 is 2^3 each digit of octal will have equivalent 3 bits of binary)

6 7 3
110 111 011

12.Convert $(3A.6)_{16}$ to binary:
A. 1110100110 B. 1010100110 C. 1100100110 D. 1110010110 E. 1110101010
Answer: A
Solution:
To convert from radix r=16 to radix r=2 we should convert digit by digit as following: (since 16 is 2^4 each digit of hexadecimal will have equivalent 4 bits of binary)

3 A 6
0011 1010 0110

13. A small-scale integration (SSI) device contains _____ gates in a single chip.
A. thousands of B. From10 to 1000 C. More than 100
D. From 10 to 100 **E. less than 10**
Answer: E
Solution:
To be a SSI, device has to have less than 10 (0 to 9) gates in a single chip

14 A very-large-scale integration (VLSI) device contains _____ gates in a single chip.
A. thousands of B. From10 to 1000 C. More than 100
D. From 10 to 100 E. less than 10
Answer: A
Solution:
To be a VLSI, device has to have more than one thousand or thousands (1000…) of gates in a single chip

15. How many functions of 2 variables do you know?
A. 4 B. 8 **C. 16** D. 24 E. 32
Answer: C
Solution:
Number of functions of variables is defined by formula 2^{2^n} - where n is number of variables.
Here we have n=2, so the number of functions is 16

16. The function $F=\sum(0,1,3,4,7)$. Expression of the function's complement is:
A. $F'=\sum(5,6)$ **B. $F'=\sum(2,5,6)$** C. $F'=\sum(0,1,3,4,7)$
D. $F'=\sum(0,1,5,6)$ E. $F'=\sum(0,2,5,6)$
Answer: B
Solution:
To find the complement of F , we simply find missed numbers in interval of 0 to 7. We see they are 2,5,6. $F'=\sum(2,5,6)$

17.Number of functions of n variables can be determined according to the formula
A. 2^{2^n} B. 2^{2n} C.2^n D.2^{3^n} E. 2^{3n}
Answer: A
Solution:
It is obvious , since it is formula - 2^{2^n} (look question 15)

18. XY'+X'Y is algebraic expression of _____ function.
A. XOR B. XNOR C. NOR D. NAND E. AND
Answer: A
Solution:
XY'+X'Y is the algebraic expression of XOR denoted by ⊕

19.7400 is IC of _____ logic family.
A. TTL B. ECL C. MOS D. CMOS E. I^2L
Answer: A
Solution:
7400 is IC of TTL family's NAND gate

20. 4000 is IC of _____ logic family.
A. TTL B. ECL C. MOS **D. CMOS** E. I^2L
Answer: D
Solution:
4000 is IC of CMOS logic family

21. Typical voltage for IC TTL logic family for positive logic is for HIGH -_____V, for LOW - _____V.
A. 0.2, 3.5 **B. 3.5, 0.2** C. 5, 0 D. 0, 5 E. 0, 3.5
Answer: B
Solution:
Typical voltage for TTL for positive logic is for HIGH is 3.5 V (as we say 1 = 5 V)and for LOW is 0.2V (as we say 0 = 0V)

22. Typical voltage for IC TTL logic family for negative logic is for HIGH -_____V, for LOW - _____V.
A. 0.2, 3.5 B. 3.5, 0.2 C. 5, 0 D. 0, 5 E. 0, 3.5
Answer: A
Solution:

Typical voltage for TTL for negative logic is for HIGH is 0.2 V and for LOW is 3.5V

23. 14 pin TTL SSI chip can contain _____ 3 input AND gates.
A. 1 B. 2 C. 3 D. 4 E. 5
Answer: C
Solution:
If chip has 14 pins, for VCC and GND one pin each is given so 12 pins left. 3 input AND gate has one output so for gate fully with input and output 4-pins are needed. 12/4=3 so we can at most 3 3-input AND gates in 14 pin TTL chip

24. A encoder is a combinational circuit that
A. converts binary information from n input lines to a maximum of 2^n unique output lines
B. has 2^n (or less) unique input lines and n output lines
C. selects binary information from one of many input lines and direct it to a single output line
D. receives information on a single line and transmits this information on one of 2^n possible output lines
E. converts binary information from n input lines to m output lines
Answer: B
Solution:
Encoder is a combinational circuit that has 2^n (or less) unique input lines and n output lines (examples: 74147,74148)

25. _____ flip-flop gives us uncertainty if set and reset inputs have value 1 at the same time.
A. RS and clocked RS B.RS or clocked RS C. D D. JK E. T

Because in RS when 1's are applied to both R and S inputs Q and Q' both will be 0's. NOR gates produce 0's when at least one 1 is applied that both of outputs are 0's which is not correct because outputs must be different 1 0 or 0 1. And in clocked RS with both R=1 and S=1, the occurrence of a clock pulse causes both outputs to momentarily go to 0.
When the pulse is removed, the state of the flip-flop is undetermined, either state may result, depending on whether the set or reset input of the basic flip-flop remains 0 1 longer the transition to 0 at the end of the pulse.

26. Master-slave flip-flop consists of _____ flip-flop(s).
A. 1 B. 2 C.1 or 2 D. 3 E. 2 or 3

Master-slave flip-flop consists of two same flip-flops called RS. Output Q of the first flip-flop connected to S input of the second flip-flop and output Q' in connected to R input of the second flip-flop.

27. A synchronous sequential circuit is a system whose behavior
A. depends upon the order in which its input signals change
B. depends upon the order in which its input signals change and can be affected at any instant of time
C. can be defined from the knowledge of its signals
D. can be defined from the knowledge of its signals at discrete instants of time
E. can be defined by sequence of pulses

Synchronous sequential logic systems use fixed amplitudes such as voltage levels for the binary signals. Synchronization is achieved by a timing device called a master-clock generator which generates a periodic train of clock pulses. The clock pulses are distributed throughout the system in such a way that memory elements are affected only with the arrival of the synchronization pulse. In practice, the clock pulses are applied into AND gates together with the signals that specify the required change in memory elements.
The AND gate outputs can transmit signals only at instant which coincide with the arrival of clock pulses.

28. Power dissipation is
A. the power consumed by the gate
B. the power consumed by the gate, which must be available from the power supply
C. the power consumed by the gate, which may be available from the power supply
D. the power emitted by the gate
E. the power emitted by the gate, which may be available for the gates of the next level

It must require power supply because this power is required to operate the gate.

29. A register is
A. a group of storage cells suitable for holding information
B. a group of storage cells suitable for holding binary information
C. a group of binary cells suitable for holding information
D. a group of binary storage cells suitable for holding binary information
E. a group of binary cells suitable for processing information

Since one binary cell can store one bit a register of n cells can store any discrete quantity of information that contain n bits.

30. A full subtractor is a _____ circuit, that performs a subtraction _____ bits, taking into account that a _____ may have been borrowed by a _____ significant stage.
A. sequential; of three; 1; higher
B. sequential; between two; carry; higher
C. combinational; between two; 1; higher
D. combinational; of three; carry; lower
E. combinational; between two; 1; lower

31. A read-only memory (ROM) is a device that includes _____ within a single IC package
A. the decoders and the OR gates
B. the decoder and the OR gates
C. the decoders and the OR gate
D. the decoders and the AND gates
E. the decoders and the NAND gates

Two connection between outputs of the decoder and the inputs of the OR gates can be specified for each particular configuration by "programming" the ROM.

32. A decoder is a combinational circuit that
A. converts binary information from n input lines to a maximum of 2^n unique output lines
B. has 2^n (or less) unique input lines and n output lines
C. selects binary information from one of many input lines and direct it to a single output line

D. receives information on a single line and transmits this information on one of 2^n possible output lines
E. converts binary information from n input lines to m output lines

Their purpose is to generate the 2n (or less) minterms of n input variables.

33. Serial binary adder consists of
A. n full adders, connected in cascade, where n-number of digits for addition
B. n half adders, connected in cascade, where n-number of digits for addition
C. n full adders and a storage device, where n-number of digits for addition
D. n half adders and a storage device, where n-number of digits for addition
E. one full adder and a storage device

Full adder is for addition of one pair of bits at a time and storage device is for storing carry out.

34. Noise margin is
A. the limit of a noise voltage
B. the limit of a noise voltage, which may be present without impairing the operation of the circuit
C. the limit of a noise voltage, which may be present without impairing the proper operation of the circuit
D. the limit of voltage, which may be present without impairing the operation of the circuit
E. the limit of voltage, which may be present without impairing the proper operation of the circuit

There are two types: DC noise is caused by a drift in the voltage levels of a signal. AC noise is a random pulse that may be created by other switching signals.

35. Counter is
A. a circuit that goes through a prescribed sequence of states
B. a sequential circuit that goes through a prescribed sequence of states
C. a circuit that goes through a prescribed sequence of states upon the application of pulses
D. a circuit that goes through a prescribed sequence of states upon the application of input pulses
E. a sequential circuit that goes through a prescribed sequence of states upon the application of input pulses

In a counter, the sequence of states may follow a binary count or any other sequence of states. The input pulses, called count pulses, may be clock pulses or any external source.

36 A half-subtractor is a _____ circuit, that subtracts _____ bits and produces their difference.
A. sequential; three
B. sequential; two
C. combinational; two
D. combinational; three
E. sequential or combinational; three

It has an output to specify if a 1 has been borrowed. To perform x-y, we have to check the relative magnitudes of x and y. If x>=y, we have three possibilities: 0-0=0,1-0=1 1-1=0.If x<y, we have 0-1, and it is necessary to borrow a 1 from the next higher stage.

37. Chip is
A. integrated circuit
B. integrated circuit, containing transistors, diodes, resistors, capacitors
C. circuit, containing transistors, diodes, resistors, capacitors
D. integrated circuit, containing photo diodes and opto couples
E. integrated circuit, containing transistors and diodes
That components called transistors, diodes, resistors, capacitors are interconnected inside the chip to form an electronic circuit.

38. Propagation delay is
A. the average transition delay time for the signal to propagate from input to output when the signals change in value
B. the average transition delay time for the signal to propagate from input to output
C. the transition delay time for the signal to propagate from input to output
D. the transition delay time for the signal to propagate from input to output when the signals change in value
E. the average transition delay time for the signal to propagate from input of one gate to input of the next gate

The signals through a gate take a certain amount of time to propogate from the inputs to the outputs. This interval of time is defined as the propogation delay.

39. A demultiplexer is a combinational circuit that
A. converts binary information from n input lines to a maximum of 2^n unique output lines
B. has 2^n (or less) unique input lines and n output lines
C. selects binary information from one of many input lines and direct it to a single output line
D. receives information on a single line and transmits this information on one of 2^n possible output lines
E. converts binary information from n input lines to m output lines

DUX works as decoder if E line is taken as a data input line. And it has selection lines for direction of data.

40. A asynchronous sequential circuit is a system whose behavior
A. depends upon the order in which its input signals change
B. depends upon the order in which its input signals change and can be affected at any instant of time
C. can be defined from the knowledge of its signals
D. can be defined from the knowledge of its signals at discrete instants of time
E. can be defined by sequence of pulses.

Answer : There are two types of sequential circuits, and their classification depends on the times at which their inputs are observed and their internal state changes. The behavior of an *asynchronous sequential circuit* depends upon inputs at any instant of time and the order in continuous time in which the inputs change.

41. Master-clock generator is
A. a timing device
B. a timing device which generates a periodic pulses
C. a timing device which generates a periodic train of pulses
D. a timing device which generates a periodic train of clock pulses
E. a timing device which generates a train of clock pulses

42. A shift register is a register which
A. capable of shifting its binary information
B. capable of shifting its binary information to the right
C. capable of shifting its binary information to the left
D. capable of shifting its binary information either to the right or to the left
E. capable of shifting its binary information either to the right and to the left

Def.: A register capable of shifting its stored bits laterally in one or both directions is called a *shift register.*

43. A bidirectional shift register is a register which
A. capable of shifting its binary information
B. capable of shifting its binary information to the right
C. capable of shifting its binary information to the left
D. capable of shifting its binary information either to the right or to the left
E. capable of shifting its binary information either to the right and to the left

Def.: A register capable in one direction only is called *unidirectional shift register.* A register that can shift in both direction is called *bidirectional shift register.*

44. Full adder forms _____, but half-adder forms _____.
A. the sum of two bits, ... the sum of two bits and a previous carry.
B. the sum of two bits, ... the sum of two bits and a carry
C. the sum of two bits, ... the sum of two bits and a present carry
D. the sum of two bits and a carry,... the sum of two bits
E. the sum of two bits and a previous carry, ... the sum of two bits

Answer : A half adder is an arithmetic that generates the sum of two binary digits. A full adder is a combinational circuit that forms the arithmetic sum of three input bits: two bits and carry.

45. Priority encoder establishes _____ to ensure that only the highest –priority input line is encoded.
A. a priority B. a line priority **C. An input priority**
D. an output priority E. a general priority

Answer: The operation of the priority encoder is such that if two or more inputs are equal to 1 at the same time, the input having the highest priority takes precedence.

46. A multiplexer is a combinational circuit that
A. converts binary information from n input lines to a maximum of 2^n unique output lines
B. has 2^n (or less) unique input lines and n output lines
C. selects binary information from one of many input lines and direct it to a single output line
D. receives information on a single line and transmits this information on one of 2^n possible output lines
E converts binary information from n input lines to m output lines

47. Parallel binary adder consists of
A. n full adders, connected in cascade, where n-number of digits for addition
B. n half adders, connected in cascade, where n-number of digits for addition
C. n full adders and a storage device, where n-number of digits for addition
D. n half adders and a storage device, where n-number of digits for addition
E. one full adder and a storage device

48. Fan-out specifies
A. the number of loads that the output of the gate can drive without impairment of its operation
B. the number of standard loads that the output of the gate can drive without impairment of its operation
C. the number of loads that the output of the gate can drive without impairment of its normal operation
D. the number of standard loads that the output of the gate can drive without impairment of its normal operation
E. the number of loads that the input of the gate can drive without impairment of its operation

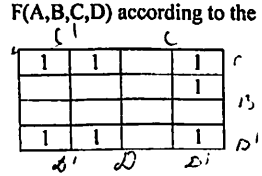
Def.: The **fan-out** of a subfamily is defined as the number of gate inputs of the same subfamily that can be connected to a single output without exceeding the current rating of the gate.

49. Positive-logic NOR gate is the same as negative-logic _____ gate.
A. OR **B. NAND** C. AND D. XOR E. XNOR

50. A majority gate is
A. a circuit whose output is equal to 1 if the majority of the inputs are 1's, otherwise the output is 0
B. a digital circuit whose output is equal to 1 if the majority of the inputs are 1's, otherwise the output is 0
C. a circuit whose output is equal to 1 if the majority of the inputs are 1's
D. a digital circuit whose output is equal to 1 if the majority of the inputs are 1's
E. a digital circuit whose output is equal to 1 if the majority of the inputs are 0's, otherwise the output is equal to 1

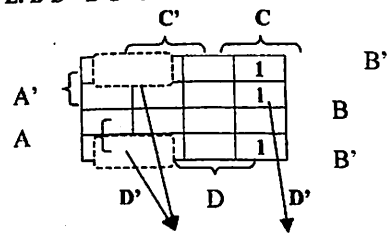
51. Simplification of the Boolean function F= (A+B)′(A′+B′)′ to a minimum number of literals is:
A. AB **B. 0** C. A+B D. A E. B
Answer : F= (A+B)′(A′+B′)′ = (A′B′) (AB) = (A′A) (B′B) = (0) (0) = 0.

52. Simplification of the function F(A,B,C,D) according to the map is:



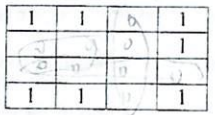
A. B′D+B′C′+A′CD′ B. B′D+B′C′+A′CD C. B′D+B′C′+ACD′
D. B′D+B′C′+A′C′D′ **E. B′D′+B′C′+A′CD′**

Solution :



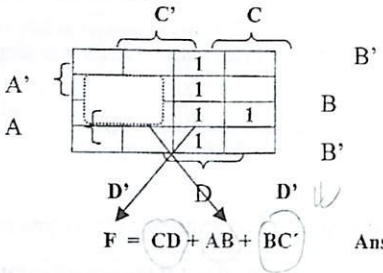
F = B'D' + B' C' + A′CD′ **Answer: E**

53. Complement of the function F(A,B,C,D) according to the map is:



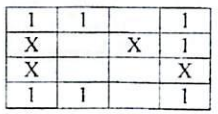
A. CD+AB+ BC′ B. C′D+AB+ BC′ C. CD+AB+ B′C
D. C′D′+AB′+B′C E. C′D′+AB′++A′BC′

Solution :



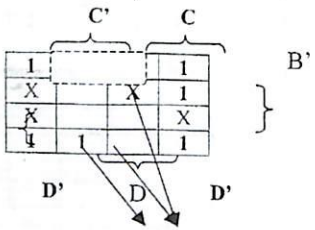
F = CD + AB + BC′ **Answer: A**

54. Simplification of the function F(A,B,C,D) according to the map is:



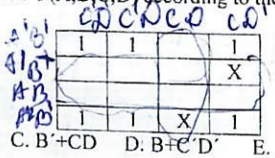
A. B′D′+B′C B. B′D+B′C′ **C. D′+B′C′** D. D+B′C′ E. B′D′+B′C′

Solution :



F = D′+B′C′ **Answer: C**

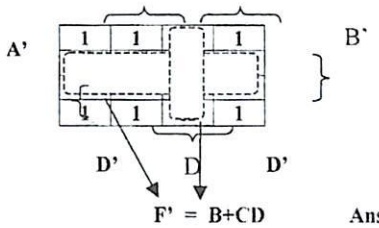
55. Complement of the function F(A,B,C,D) according to the map is:



A. B+CD′ B. B′+C′D C. B′+CD D. B+C′D′ E. B+CD

Solution :

C' C



F' = B+CD **Answer: E**

56. Applying tabulation method we can match _____ with 0010:
A. 1010 B. 0111 C. 1110 D. 0101 E. 1011

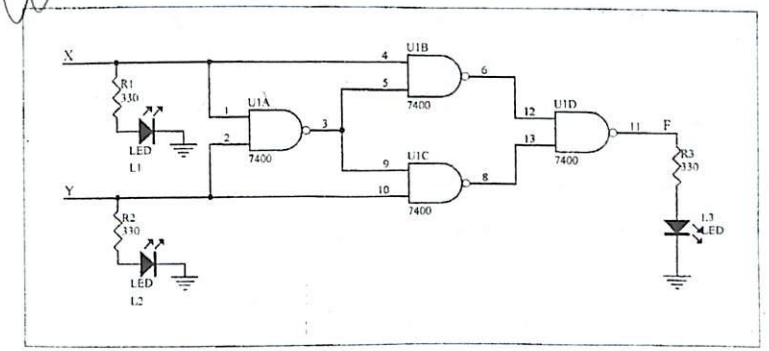
True answer is: A. 1010 **In tabulation method only one digit may be differ**

0010 – 1010

57. Canonical form of a function's representation can give us its _____ level implementation.
A. 1 **B. 2** C. 1 or 2 D. 3 E. 2 or 3

Answer: In canonical form,(product of sums or sum of products) can give us 2 level implementation

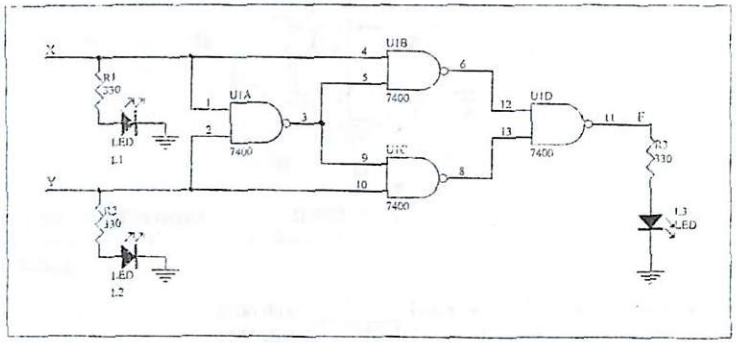
58. What is the output of U1A in the figure?



A. XY B. X+Y C. (X+Y)′ D. X′+Y′ **E. (XY)′**

Answer: U1A is NAND gate, so NOT(X AND Y) = (XY)'

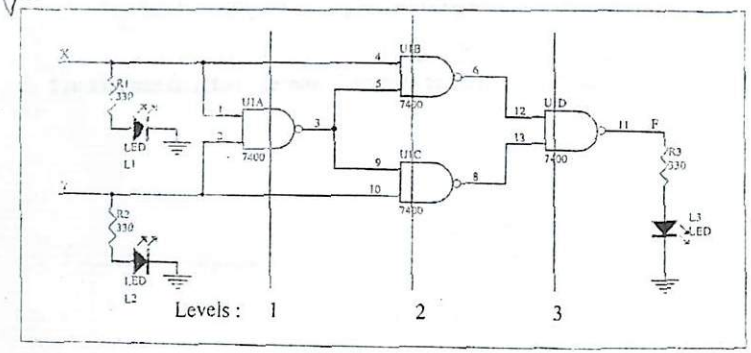
59. Propagation delay of NAND gate in the figure is 10ns. What is propagation delay of the output F of the circuit?



A. 10ns B. 20ns **C. 30ns** D. 40ns E. 50ns

Answer: in implementation above 3 levels so 3*10ns= 30ns

60. How many levels of implementation the scheme in the figure has?



A. 1 B. 2 **C. 3** D. 4 E. 5

61. Which function is in its standard form?

A. A+B(C+D) **B. A+BC** C. (AB+ CD)(A+C) D. (A+B)(CD+AB′)

E. (A B′+CD)(AB′+C′D)

Answer: standard form is product-of-sums or sums-of-products

62. We have got the map:

A \ B	X	1	X	X
X		1	1	X

C

Simplified function is equal to:

A. C B. A+C′ **C. 1** D. A′+AC E. B+ B′C

63. Multiplication of two binary numbers (11 and 11) equals to:

A. 1010 B. 0111 C. 1101 D. 1011 **E. 1001**

```
  11
 *11
 --
  11
+11
----
1001
```

64. 1's complement of binary number of 10011 is equal to:

A. 01100 B. 01101 C. 10010 D. 01110 E. 10001

Answer: 1's complement is inverse of number, change all 1's to 0's and vise versa.

65. A magnitude comparator is a _____ circuit, which determines whether

A. Combinational; A>B, A=B, or A<B.

B. Combinational; A>B, A=B, and A<B.

C. Sequential; A>B, A=B, or A<B.

D. Sequential; A>B, A=B, and A<B.

E. Combinational or sequential; A>B, A=B, or A<B.

Answer: A magnitude comparator is a combination circuit, which give result of comparison greater, smaller, or equal.

66. What statement is wrong?

A. X+X′=1 B.X+0=X C. X*1=X D. X*X′=0 **E.X+1=X**

Answer: X+1=1

67. Which function is in canonical form?

A. (AB+CD)(A′B′+C′D) B. (ABC+C′D)(A+E) C. (ABC+CD)(AE+BC)

D. (A+BE)(BC+DE) **E. (A+B+C+D′)(A′+B+ C′+D)**

Answer: canonical form is product-of-sums

68. According to the truth table function F_1 is equal to function _____

X	Y	Z	F_1	F_2	F_3	F_4	F_5	F_6
0	0	0	1	1	1	1	1	0
0	0	1	0	1	0	0	0	0
0	1	0	1	1	0	1	1	1
0	1	1	0	0	0	0	1	0
1	0	0	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0

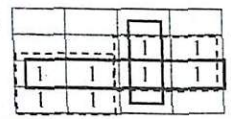
A. $F_1 = F_2$ B. $F_1 = F_3$ **C. $F_1 = F_4$** D. $F_1 = F_5$ E. $F_1 = F_6$

69. Simplification of the Boolean function F=BC+AC′+AB+BCD to a minimum number of literals gives us:

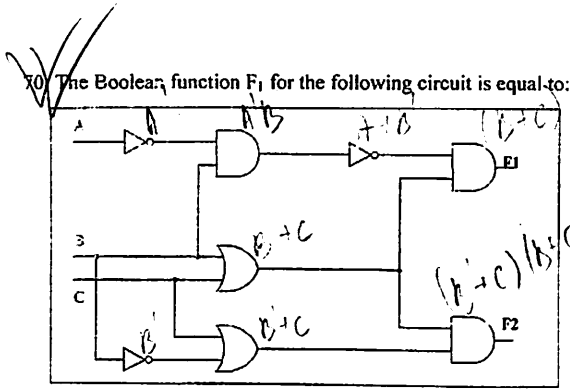
A. BC+AC B. B+AC C. BC+A D. BC+AB **E. BC+AC′**

Solution: function F=BC+AC′+AB+BCD on Karnaugh map is represented as:

Where it may be simplifies as BC+AC'



70. The Boolean function F_1 for the following circuit is equal to:



A. (A+B′)(B+C) B. (A+B)(B′+C) C. (A+C)(B′+C) D. C E. B+C

Solution: inputs for AND gate of F1 are (B+C) and inverted (A'B), result: (A+B')(B+C)

71. What fragment corresponds to definition of the Gray code?

A		
x	y	F
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

B		
x	y	F
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1

C		
x	y	F
0	0	0
0	0	1
0	1	1
0	1	0
1	0	0

D		
x	y	F
0	0	0
1	0	0
1	0	1
1	1	0
1	1	1

E		
x	y	F
0	0	0
1	0	0
1	1	1
1	1	0
1	0	1

Solution: Gray code is binary coding system where each successive binary string within the code changes by only 1 bit.

72. Binary subtraction of 10011010-00110110 gives us:
A. 10011100 B. 1000100 **C. 01100100** D. 10100100 E. 11000100

Solution: column:

	10011010
−	00110110
	01100100

where 1 may be borrowed from next-more-significant

When it borrows from its left, it increases by 2.

73. Subtraction $(345)_8$-$(256)_8$ gives us:
A. 57 B. 66 C. 56 D. 156 **E. 67**

Solution: Subtraction of octal numbers is similar to decimal subtraction except that, when you borrow 1 from the left, the borrower increases in value by 8. in this example, we cannot subtract 6 from 5, so the 5 borrows 1 from 4. This changes 4 to 3, and 5 increases in value by 8 (5+8=13). Now, 13-6=7, and 5 cannot be subtracted from 3, 3 borrows 1 from higher significant digit (3+8=11), then 11-5=6, remains 2-2=0; result: 67.

74. A feedback path is a connection from the output of one gate. To

A. the output of a second gate B the input of a second gate
C. the input of a second gate that forms part of the input to the first gate
D. the input of a second gate that forms part of the input to the second gate
E. the output of a second gate that forms part of the input to the first gate

75. A code converter is a circuit that
A. makes the several systems compatible
B. makes the two systems compatible
C. makes the two systems compatible even though each uses a different binary code
D. makes the two systems compatible even though each uses different codes
E. makes the several systems compatible even though each uses different binary codes

76. The 15's complement of $(AB6)_{16}$ is equal to
A. 348 B. 349 C. 439 D. 538 **E. 549**

Solution: Easiest solution is to subtract digit from "15": (15-6)=9, (15-B)=(15-11)=4, (15-A)=(15-10)=5, result: 549

77. A combinational circuit consists of
A. input and output variables
B. logic gates
C. logic gates with feedback
D. input variables, logic gates, and output variables
E. input variables, logic gates with feedback, and output variables

78. A binary parallel adder is a digital function that produces:
A. the sum of two binary numbers
B. the arithmetic sum of two binary numbers
C. the sum of two binary numbers in parallel
D. the arithmetic sum of two binary numbers in parallel
E. the sum of two binary numbers and carry in parallel

79. What are don't care conditions for the function F=A′B′C′D+A′BC+AB′C if its simplification gives us F=A′C+B′C+A′B′?
A. d=A′B′+A′D B. d=A′C′+A′D **C. d=A′B′C+A′B′D′**
D. d=A′B′C+A′D E. d=A′B′C+A′BD′

x	1	x	x
		1	1
		1	1

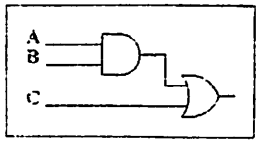
Solution: function F=A′B′C′D+A′BC+AB′C is represented as And simplified form F=A′C+B′C+A′B′
x- Don't care conditions

1	1	1	1
		1	1
		1	1

80. Subtraction D7-A8 in hex gives us:
A. 3E B. 2D C. 3D **D. 2F** E. 3F

Solution: Subtraction of hexadecimal numbers is similar to decimal subtraction except that, when you borrow 1 from the left, the borrower increases in value by 16.

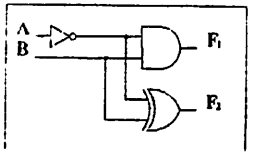
81. The following circuit can be implemented with ____ NAND gates (all normal and complemented inputs are available).



A. 1 B. 2 C. 3 D. 4 E. 5

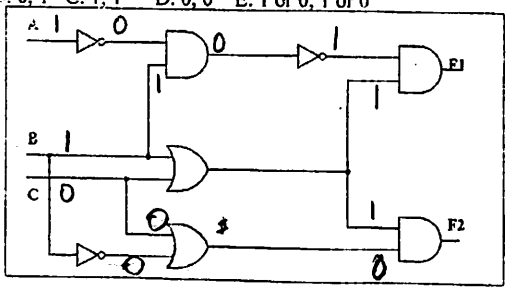
Solution: equation of the circuit is AB+C, taking into consideration that complementing inputs are available, our equation is equivalent to [(AB)'.C']', where first NAND gate in ()-braces, the second is in []-brackets.

82. This circuit is



A. full-adder B. Half-adder C. Full-subtractor D. Half-subtractor
E. none of the above mentioned

83 If A=1, B=1,C=0, F_1 and F_2 equals to _____ respectively.
A. 1, 0 B. 0, 1 C. 1, 1 D. 0, 0 E. 1 or 0, 1 or 0



Solution: According to the circuit F1= (A'B)'(B+C) or (A+B')(B+C), and F2= (B+C)(B'+C) or (C)
By applying the given inputs you gain 1 and 0 respectively.

84. A parity generator is a circuit, that
A. receives the parity bit
B. receives the parity bit from the transmitter
C. **generates the parity bit in the transmitter**
D. generates the parity bit
E. generates the parity bit for the transmitter

Solution:
The parity system adds an extra bit to the digital information being transmitted. The parity generator is the circuit that creates the parity bit. So, the answer is **C.**

85. A parity checker is a circuit, that
A. receives the parity bit
B. receives the parity bit from the transmitter
C. check the parity bit
D. check the parity bit in the transmitter
E. check the parity in the receiver

Solution:
The parity system adds an extra bit to the digital information being transmitted. On the receiving end, a parity checker determines if the result is of the right parity. So, the answer is **E.**

86. A parity bit is an extra bit included with
A. a binary message to make the number of 1's either odd or even
B a binary message to make the number of 0's either odd or even
C a message to make the number of 1's either odd or even
D a binary message to make the number of 1's odd
E a binary message to make the number of 1's even

Solution:
Here it is obvious that answer is **A.**

87. The operator _____ is called unary operator.
A. XOR B. AND C. OR D. XNOR **E. NOT**

Solution:
AND, OR are binary operators. But NOT is unary operator.

88. The operator _____ is called binary operator.
A. XOR B. buffer **C. OR** D. XNOR E. NOT

89. Operation OR can be represented by_____ NAND gate(s).
A. 1 B. 2 C. 1 or 2 **D. 3** E. 2 or 3

Solution:
First NAND gate we use to take the complement of first input. Second NAND gate we use to take the complement of second input. And third NAND gate we use to take NAND of two complemented inputs. Then result will be OR.

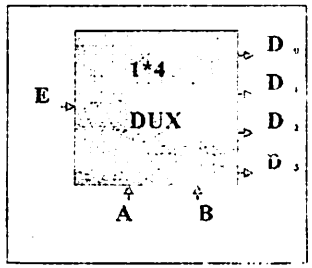
90. Operation AND can be represented by_____ NOR gate(s).
A. 1 B. 2 C. 1 or 2 **D. 3** E. 2 or 3

Solution:
First NOR gate we use to take the complement of first input. Second NOR gate we use to take the complement of second input. And third NOR gate we use to take NOR of two complemented inputs. Then result will be AND.

91. For priority encoder we have got input lines D_1, D_2, and D_5 active simultaneously. In such case output signal will be corresponded to …
A. D_1 B. D_2 **C. D_5** D. D_1or D_2 E. D_2 or D_5

Solution:
Priority encoder means that if more than one decimal number is input, the highest numeric input has priority and will be encoded to the output.

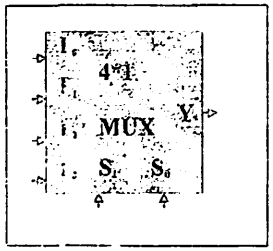
92. What output of 1*4 demultiplexer will be chosen if selection lines AB=10?



A. D_1 B. D_0 C. D_2 D. D_3 E. any of them

Solution:
AB=00 → D_0
AB=01 → D_1
AB=10 → D_2
AB=11 → D_3

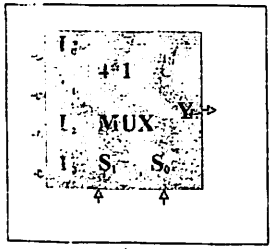
93. What will the output signal of 4*1 multiplexer be if selection lines S_1S_0=11?



A. I_0 B. I_1 C. I_2 **D. I_3** E. any of them

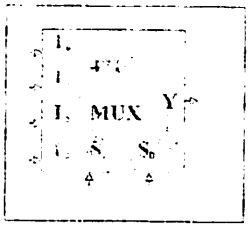
Solution:
S_1S_0=00 → I_0
S_1S_0=01 → I_1
S_1S_0=10 → I_2
S_1S_0=11 → I_3

94. What will the output signal of 4*1 multiplexer be if selection lines S_1S_0=00?



A. I_0 B. I_1 C. I_2 D. I_3 E. any of them

Solution:
S_1S_0=00 → I_0
S_1S_0=01 → I_1
S_1S_0=10 → I_2
S_1S_0=11 → I_3



A. I_0 **B. I_1** C. I_2 D. I_3 E. any of them

Solution:
S_1S_0=00 → I_0
S_1S_0=01 → I_1
S_1S_0=10 → I_2
S_1S_0=11 → I_3

96. For odd-parity checker the error is in the _____ row.

# of row	Four-bits received				Parity-error check
	x	y	Z	P	C
1	0	0	0	1	0
2	0	1	0	0	0
3	1	0	1	1	0
4	0	0	1	1	1
5	1	1	1	0	0

A. 1 B. 2 C. 3 **D.4** E.5

Solution:
Parity-error check gives 1 when it finds error.

97. For even-parity checker the error is in the _____ row.

# of row	Four-bits received				Parity-error check
	x	y	Z	P	C
1	0	0	0	0	0
2	0	1	0	1	0
3	1	0	1	0	0
4	0	0	1	1	0
5	1	1	1	0	1

A. 1 B. 2 C. 3 D.4 **E.5**

Solution:
Parity-error check gives 1 when it finds error.

98. An algorithm is

A. a set of steps to obtain the result
B. a procedure to obtain the result
C. a procedure that specifies a set of steps
D. a procedure that specifies a finite set of steps which, if followed, give the solution of the problem
E. a procedure that specifies a set of steps which, if followed, give the solution of the problem

Solution:
An algorithm is a procedure that specifies a finite set of steps which, if followed, give the solution of the problem.

99. A multiplexer is called a data selector, since it selects
A. inputs and steers the binary information to the outputs
B. one of many inputs and steers the binary information to the output line
C. one of many inputs and steers the binary information to the outputs
D. inputs and steers the binary information to the output line
E. one of many inputs and steers the binary information to many of the outputs

Solution:
A multiplexer is called a data selector, since it selects one of many inputs and steers the binary information to the output line.

100. MUX can realize _____ function(s).
A. 1 B. 2 C. 3 D. 4 E. any number of

Solution:
Because it selects one of many inputs and steers the binary information to the output line.

101. For BCD addition for correction we add
A. 1001 B. 0110 C. 1100 D. 0101 E none of them

For BCD addition for correction we add 0110 to pass through unused states 10,11,12,13,14,15 total 6 unused states.

102. This is characteristic table of _____ flip-flop.

		Q (t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	?

A. RS B. set-dominate RS C. D D. JK E. T

The following is the characteristic table of RS flip-flop by definition

103. This is excitation table of _____ flip-flop.

Q(t)	Q (t+1)		
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

A. RS B. set-dominate RS C. D D. JK E. T

The following is the excitation table of RS flip-flop by definition

104. What state sequence for Q(t+1) is correct?

J	K	Q (t+1)
0	0	
0	1	
1	0	
1	1	

A. 1, 0, Q(t), ? B. 1, 0, ?, Q(t) C. Q(t), 0,1,Q'(t) D. Q(t), 0,1, 1 E. Q(t), 0,1, 0

The Q(t+1) at J=0,K=0 is Q(t) (no change) , at J=0 K=1 it is 0(reset) , J=1 K=0 it is 1(set) and
J=1 K=1 it is Q'(t) so the sequence will be Q(t),0,1,Q'(t).

105. What state sequence for input S is correct?

Q(t)	Q (t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

A. 0,1,1,0 B. 0,1,1,X C. 1,0,0,X D. 0,1,0,1 E. 0,1,0,X

Using excitation table for SR flip-flop we can easily see that sequence for S will be 0,1,0,x

106. What state sequence for input J is correct?

Q(t)	Q (t+1)	J	K
0	0		X
0	1		X
1	0		1
1	1		0

A. 0,1,1,X B. 0,1,X,X C. 1,0,0,X D. X,0,1,0 E. 0,1,0,X

Using excitation table for JK flip-flop we can easily see that the sequence for input is 0,1,x,x

107. A set-dominate flip-flop differs from a conventional _____ one in that an attempt to _____ results in _____ the flip-flop.

A. JK, simultaneously set and reset, setting
B. JK, set and reset, setting
C. RS, simultaneously set and reset, setting
D. RS, set and reset, setting
E. RS, simultaneously set and reset, resetting

By definition Set Dominate flip-flop differs from conventional SR one in that an attempt to simultaneously set and reset result in setting the flip-flop

108. Next state of flip-flop is a function of
A. present state
B. Present state and the inputs
C. the inputs and the type of flip-flop used
D. Present state and the type of flip-flop used
E. the inputs, the present state and the type of flip-flop used

Next state of flip-flop depends on the inputs the present state and the type of flip-flop used

109. The state diagram of the sequential circuit
A. consists of circles and lines
B. is another view of the state table
C. is graphical representation of the state table
D. contains additional information about sequential circuit
E. shows only present state of the sequential circuit

The state diagram by definition is graphical representation of state table

110. A state equation of the sequential circuit is
A. an expression to describe next state of the circuit
B. an expression to describe present state of the circuit
C. a Boolean function that specifies the present state conditions
D. a Boolean function that specifies the present state conditions that make the next state equal to 1
E. a Boolean function that specifies the next state conditions that make the present state equal to 1

A state equation of the sequential circuit a Boolean function that specifies the present state conditions that make the next state equal to 1

111. Function # _____ corresponds to function NOR of 3 variables.

X	Y	Z	F_1	F_2	F_3	F_4	F_5
0	0	0	0	0	0	0	1
0	0	1	0	0	1	1	0
0	1	0	0	0	1	1	0
0	1	1	1	1	1	1	0
1	0	0	0	1	1	1	0
1	0	1	1	1	1	1	0
1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	0

A. 1 B. 2 C. 3 D. 4 E. 5

Function #5 corresponds to function NOR of 3 variables by truth table

x	y	z
0	0	1
0	1	0
1	0	0
1	1	0

112. What is the state equation for B(t+1) for the state table below?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	0
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	1

A. B(t+1)=ABX B. B(t+1)=ABX+ABX' C. B(t+1)=ABX+A'(B+X')
D. B(t+1)=A'B'X' E. B(t+1)=A'B'X'+AB

For the state table the present equation is B(t+1)=A'B'X'+AB
We have 000,110,111, then by map we find equation

1			
		1	1

113. State equation for A flip-flop is A(t+1)=AB+A'B'. Define correct state table for A.

Present state		Next state of A									
		1		2		3		4		5	
A	B	X=0	X=1	X=0	X=1	X=0	X=1	X=0	X=1	X=0	X=1
0	0	1	0	1	0	0	0	1	0	1	1
0	1	1	0	1	0	1	0	0	0	0	0
1	0	0	0	1	0	1	0	0	0	0	0
1	1	0	1	0	1	0	1	0	1	1	1

A. column 1 B. Column 2 C. Column3 D. Column 4 E. column 5

State equation for A flip-flop is A(t+1)=AB+A'B' and correct state table is column 5.
We have following sequence of numbers 000,110,001,111 and then use the map

1	1		
		1	1

114. Direct preset input of flip-flop is used
A. to set the flip-flop to an initial state B. to set the flip-flop
C. to set the flip-flop asynchronously
D. to set the flip-flop asynchronously during clock pulse occurrence
(E) to set the flip-flop asynchronously on a positive (or negative) value of the input signal

Direct preset input of flip-flop is used for setting asynchronously, they affect on a positive(or negative) value of the input signal without the need of clock pulse, useful for bringing all flip-flops to an initial state prior to their clocked operation.

115. Direct clear input of flip-flop is used
A. to clear the flip-flop to an initial state B. to clear the flip-flop
C. to clear the flip-flop asynchronously
D. to clear the flip-flop asynchronously during clock pulse occurrence
(E) to clear the flip-flop asynchronously on a positive (or negative) value of the input signal

Direct clear input of flip-flop is used for setting asynchronously, they affect on a positive(or negative) value of the input signal without the need of clock pulse, useful for bringing all flip-flops to an initial state prior to their clocked operation

116. How many options to gain state 11 will the circuit with the state table below have?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	0

(A.) B. 2 C. 3 D. 4 E. 5

1 option to gain 11 we see from table 00→11 when x=1

117. Resistor has got 4 strips on its case. They are situated from the left to the right in such order: yellow, blue, red, golden. What is the nominal value of resistance?
A. 220 Ω B. 1kΩ C. 330 Ω (D. 4.6 kΩ E. 10 kΩ

From the table yellow, blue, red and golden means 4.6 kΩ

118. Value of resistance is 47 kΩ. It means that the first three strips on the resistance case (in whole the case has got 4 strips) are:
A red, green, red B. Red, brown, black (C.) Yellow, violet, orange
D. yellow, black, brown E. brown, black, orange

From the table yellow, violet and orange make 47 kΩ.

119. Present state of the flip-flops AB=00. Sequence of inputs is x=1,1,0. What will be the sequence of next states of the circuit with the state table below?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	0

A. 01,00,01 B. 10,00,01 C. 11,10,00 D. 10,00,00 E. 00,01,01

Present state 00 -> 11
11 -> 10
10 -> 00
Answer: C) 11,10,00

120. It needs to convert JK flip-flop into D flip-flop. For this purpose we must

A. connect J and K inputs together B. Use inverter for J input
C. use inverter for K input
D. use inverter for J input and connect inverter's input with K input
(E.) use inverter for K input and connect inverter's input with J input

To convert D flip-flop into JK first use inverter for K input then connect inverter's input with J input
Answer: E

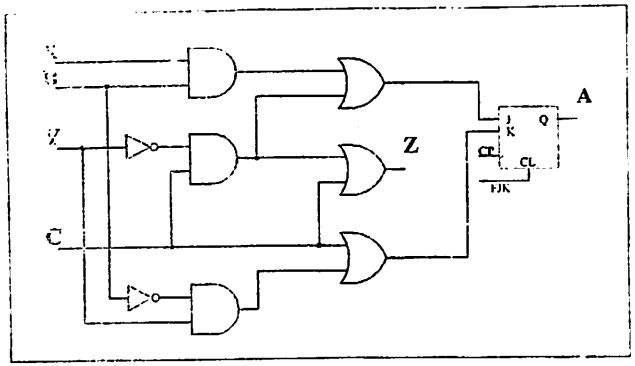
121. For the state table below define the values of T_{A1} column.

A1	A0	T_{A1}	T_{A0}
0	0		1
0	1		1
1	0		1
1	1		1

A. 1,0,1,0 (B.) 0,1,0,1 C. 1,0,0,1 D. 0,1,1,0 E. 1,1,0,0

By the excitation table of T flip_flop
00->0
01->1
11->0
10->1
Answer: B) 0,1,0,1

122. How many levels of implementation the combinational part of the circuit below has?
A. 1 B. 2 (C.) 3 D. 4 E. 5



Since the electrical signal passes through 3 gates the levels of implementation are 3
Answer : C) 3

123. We have got function F (A,B,C). We want to implement it with multiplexer. If selection lines are A and B the table for expansion on C is:

A

	I_0	I_1	I_2	I_3
C`	0	1	2	3
C	4	5	6	7

B

	I_0	I_1	I_2	I_3
C`	0	1	4	5
C	2	3	6	7

C

	I_0	I_1	I_2	I_3
C`	0	2	4	6
C	1	3	5	7

D

	I_0	I_1	I_2	I_3
C`	0	1	2	6
C	3	4	5	7

E

	I_0	I_1	I_2	I_3
C`	0	1	3	6
C	2	4	5	7

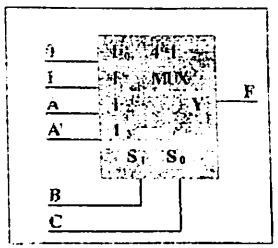
If selection lines A and B then the expansion table for C is

C

	I_0	I_1	I_2	I_3
C`	0	2	4	6
C	1	3	5	7

Answer : C

124. What function is implemented with multiplexer?



A'0(1)2(3)
A 4(5)(6)7
C 1 A A'

A. F(A,B,C)=Σ(2,3,5,6)

(B.) F(A,B,C)=Σ(1,3,5,6)

C. F(A,B,C)=Σ(2,3,5,7)

D. F(A,B,C)=Σ(2,3,6,7)

E. F(A,B,C)=Σ(1,3,5,7)

The selection lines are B and C. So we use expansion table for A

	I_0	I_1	I_2	I_3
A'	0	1	2	3
A	4	5	6	7
	0	1	A	A'

From the table we can see F(A,B,C)=Σ(1,3,5,7)
Answer: E (B)

125. The two sequential circuits are said to be equivalent if

A. identical input sequences are applied to the two circuits
(B.) identical input sequences are applied to the two circuits and identical outputs occur for all input sequences
C. identical outputs occur for all input sequences
D. input and output sequences are equal
E. all above statements are wrong

Definition: identical circuits apply identical input sequences and identical outputs occur for all input sequences

126. To multiply $B_3B_2B_1B_0$ by $A_2A_1A_0$ it needs to use _____ 4-bit parallel full-adders.
A. 1 (B.) 2 C. 3 D. 4 E. 5

To multiply 2 4 bit parallel full-adders are needed. Because we multiply 2 sequences with maximum 4 bit digits

127. For the circuit with the state table below we used D flip-flops. Show the sequence of next states of flip-flop A if D_A=AX+BX, if X=1.
A. 0,1,0,1 B.1,0,0,0 (C.) 0,1,1,1 D.0,0,0,0 E.0,1,1,0

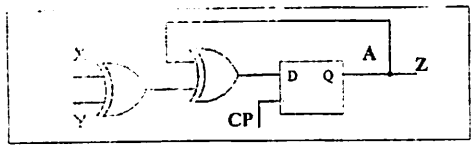
For X=1 D_A=AX+BX.

A	B	D_A
0	0	0
0	1	1
1	0	1
1	1	1

Present state		Next state				Output	
		X=0		X=1		X=0	X=1
A	B	A	B	A	B	Y	Y
0	0	0	0		1	0	0
0	1	0	0		1	1	0
1	0	0	0		0	1	0
1	1	0	0		0	1	0

_____, PLA is a device of _____, 3*8 decoder is a device of ____.
A. SSI, SSI, SSI B. SSI, SSI, MSI C. LSI, LSI, MSI D. LSI, MSI, MSI E. LSI, MSI, MSI

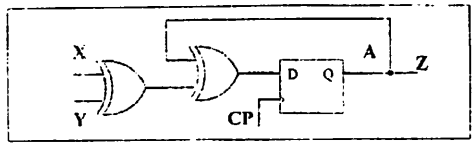
129. What is the state equation for D flip-flop for the circuit below?



A. A+X
B. A⊕X
C. A⊕X⊕Y
D. X⊕Y
E. X⊕Y⊙A

First A⊕X. Then signal goes to the next XOR and XOR with A

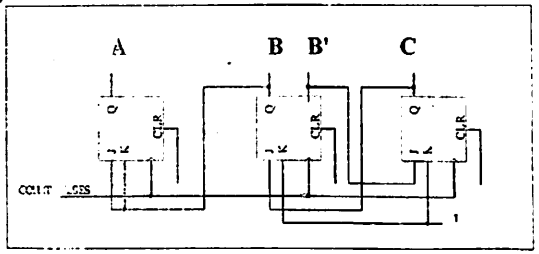
130. What is the state equation for D flip-flop for the circuit below?



A. A+X
B. A⊕X
C. A⊕X⊕Y
D. X⊕Y
E. X⊕Y⊙A

For D flip-flop state and input equations are same A⊕X⊕Y

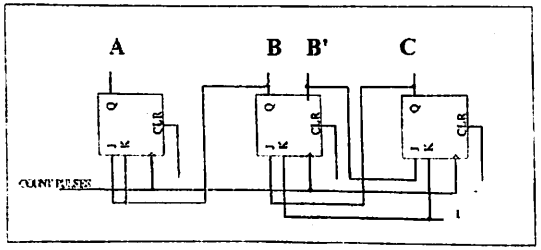
131. What is K_A input equation for the circuit below? K_A = 1



A. B'
B. B
C. A
D. A'
E. 1

The input of the K_A is the output of K_B

132. What is the state of ABC for the circuit below after the third count pulse if the initial state was 010.



A. 100
B. 101
C. 110
D. 111
E. 011

1 0 1
1 1 0

133. For the table below the sequence for J_A is
A. X,X,X,0,0,1 B. 0,0,1,X,X,X C. 0,1,X,0,1,X D. X,X,1,X,X,1 E. 1,1,0,1,0,0

Count sequence			Flip-flop inputs					
A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0		X	0	X	1	X
0	0	1		X	1	X	X	1
0	1	0		X	X	1	0	X
1	0	0		0	0	X	1	X
1	0	1		0	1	X	X	1
1	1	0		1	X	1	0	X

By the excitation table of JK flip-flop

A	B	J_A
0	0	0
0	0	0
0	1	1
1	1	X
1	1	X
1	0	X

134. What statement is correct?
A. Number of different functions of two variables is equal to 8.
B. When the number of variables in a function is odd, the minterms with an even number of 0's are the same as the minterms with an odd number of 1's.
C. NOT is a binary operator
D. Tabulation method is not applicable for functions of 4 variables
E. Decoder with enable can be used as multiplexer

Definition: When the number of variables in a function is odd, the minterms with an even number of 0's are the same as the minterms with an odd number of 1's

135. The transfer a new information into register is called _____ of register.
A. triggering B. Loading C. Set D. Reset E. none of above mentioned

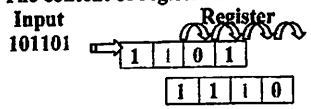
Definition: Always the transfer of new information into register is called Loading of register

136. A digital system is said to operate in _____ when information is transferred and _____ one bit at a time. The content of one register is transferred to another by _____ the bits from one register to the other.
A. a serial mode ....manipulated .... loading
B. A parallel mode ..... manipulated ....shifting
C. a serial mode ....manipulated .... shifting
D. a serial mode ....shifted .... loading
E. a parallel mode ....shifted .... Loading

Definition: A digital system is said to operate in a serial mode when information is transferred and manipulated one bit at a time. The content of one register is transferred to another by shifting the bits from one register to another.

137. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the right, with the serial input being 101101. What is the content of the register after the first shift?
A. 0101 B. 1100 C. 1110 D. 1101 E. 1010

A 4-bit shift register is initially 1101.It is shifted to the right by the serial input 101101
The content of register after the first shift will be 1110 because



138. How many flip-flops must be complemented in a 10-bit binary ripple counter to reach the next count after 0111111111?
A. 2 B. 4 C.6 D. 8 E. 10

To reach the next count of 10-bit binary ripple counter with the 0111111111 state we have to add 1 to this count so,

The count 0111111111
Next state 1
Result 1000000000

The data changed to complement it means that the 10 flip-flops must be complemented.

139. A flip-flop has a 20-ns delay from the time its CP input goes from 1 to 0 to the time the output is complemented. What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops? What is the maximum frequency the counter can operate at reliably?
A. 5 MHz B. 6.25 MHz C. 8.33 MHz D. 10 MHz E. 12.25 MHz

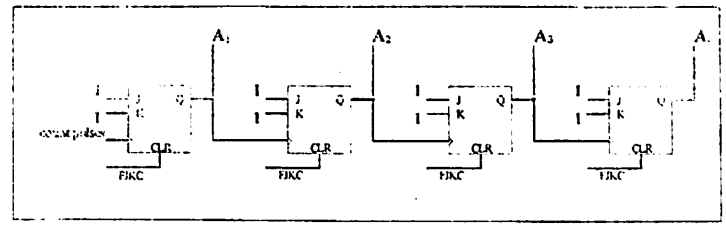
Since the flip-flop has 20-ns delay from the time its CP inputs goes from 1 to 0 .The maximum delay in a10-bit binary ripple counter is
From the formula:
T=1/F and the result is 1/ (20-ns * 10) equals to 5MHz

140. What types of operation bidirectional shift register with parallel load has?
A. shift right, parallel load B. shift left, parallel load
C. shift right, shift left, parallel load D. Complement, no change
E. shift right, shift left, parallel load, no change

Table 7-2 Function table for the bidirectional register

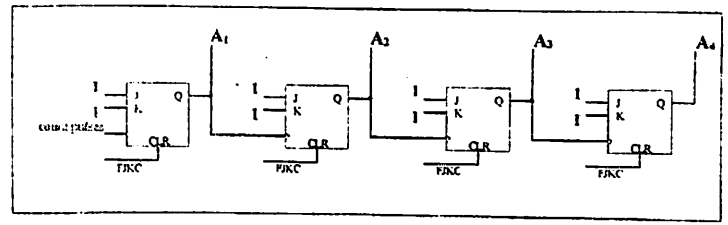
Mode Control S1	S0	Register operation
0	0	No change
0	1	Shift Fight
1	0	Shift Left
1	1	Parallel Load

141. The circuit below can count _____.
A. up B. down C. up and down D. None E. It is not a counter



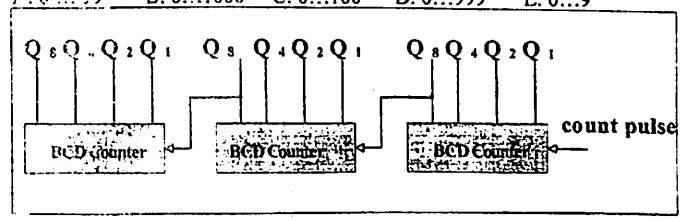
This circuit counts up, because the outputs are taken from Q, not from the Q'.

142. In what case the circuit below can count down?
A. if the outputs are taken from the complement terminals Q' of all flip-flops
B. if we apply 1's to all J inputs
C. if we apply 0's to all J inputs
D. if we apply 1's to all K inputs
E. if we apply 0's to all K inputs



If the outputs are taken from the Q', this mean that the circuit counts down!!!

143. The circuit below can count from _____ to _____.
A. 0 ... 99 B. 0...1000 C. 0...100 D. 0...999 E. 0...9



This circuit counts from 0 to 999. (0...999)
Because it is a BCD counter, let me remind you that the BCD Counter starts to count from 0000 to 1001 it are same as the decimal number representation. Since there are three counters we can see it like a first (most significant) counter as (data)*10'2 + second as (data)*10'1 + third (least significant) as (data)*10'0

144. Floating-point representation of numbers needs ____ registers.
A. 1 B. 2 C. 3 D. 1 or 2 E. 2 or 3

Definition: Floating number representation can be shown by 2 registers.

145. The XOR microoperation can be used to _____ bits of a register.
A. set B. clear C. selectively set D. Selectively clear E. selectively complement

The XOR micro operation can be used to selectively complement. Let us see the truth table:

A	B	AXORB
0	0	0
0	1	1
1	0	1
1	1	0

if we XOR data with 0 it gives 0 else with 1 it gives 1

146. The OR microoperation can be used to _____ bits of a register.
A. set B. clear C. selectively set D. Selectively clear E. selectively complement

By definition OR micro operation can be used to selectively set bits of a register

147. NOR is dual to
A. XOR B. XNOR C. NOR D. NAND E. AND

NOR is dual to NAND by definition

148. OR is complement to
A. XOR B. XNOR C. NOR D. NAND E. AND

Answer: OR is complement to NOR by definition

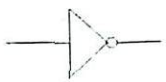
A	B	OR
0	0	0
0	1	0
1	0	0
1	1	1

A	B	NOR
0	0	1
0	1	1
1	0	1
1	1	0

149. A buffer produces the _____ function.
A. complement B.dual C. transfer D. inhibition E. implication

Answer: A buffer by definition produces the transfer function

150. Inverter can have _____ input (s).
A. 1 B.2 C. 3 D.4 E. A lot of

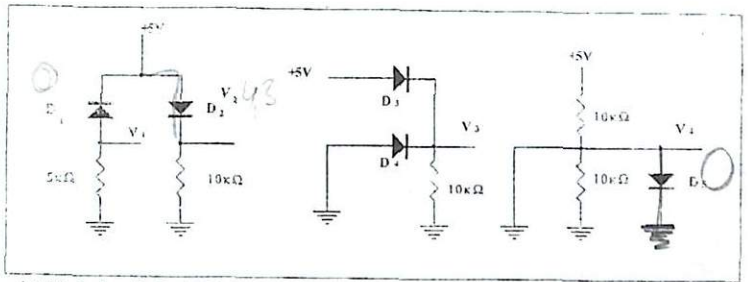


Answer: An inverter by definition can have only one input

151. Duality principle states that every algebraic expression
A. remains valid if the operators and identity elements are changed.
B. remains valid if the operators and identity elements are interchanged.
C. deducible from the postulates of Boolean algebra remains valid if the operators and identity elements are changed.
D. deducible from the postulates of Boolean algebra remains valid if the operators and identity elements are interchanged.
E.deducible from the postulates of Boolean algebra remains valid if the operators are changed.

Answer: By definition duality principle states that every algebraic expression deducible from the postulates of Boolean algebra remains valid if the operators are interchanged

152. Voltages V_1, V_2, V_4 in the scheme below equal to _____ respectively.



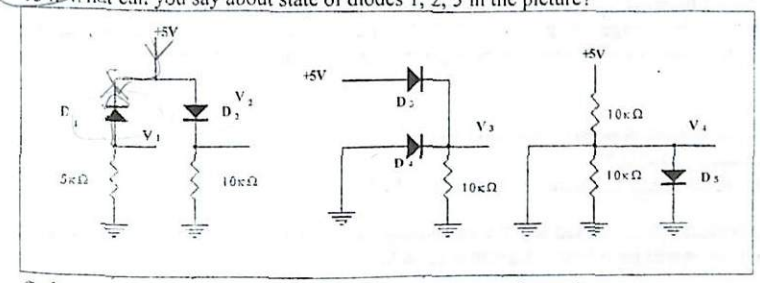
A. 4.3 V, 0, 0 B. 0, 4.3V, 0 C. 4.3 V, 4.3 V, 0 D. 0, 0, 0 E. 4.3 V, 0, 4.3 V

Answer: Since D1 reverse biased the +5V will not go through it so the V_1 will be 0V. D_2 is forward biased the +5V will pass through it and since the voltage gone (0.7V) of diode . The V_2 will be 4.3 V. V_4 is directly connected to ground so the voltage on it will be equal to 0V.

153. How many states has the switch got?
A. 1 B. 2 C. 3 D. 4 E. 5

Answer : The switch by definition has got two states which are ON and OFF.

154. What can you say about state of diodes 1, 2, 3 in the picture?



C. forward, reverse, forward D. Reverse, reverse, forward
E. forward, forward, reverse

Answer: Since anode voltage of D_1 is less than cathode voltage .the diode is reverse biased. D_2 has on it is anode voltage bigger than on it is cathode, so the diode is forward biased. D_3 is also forward biased because it is anode is connected to V_{cc} and it is cathode is on ground.

155. Analyze the information. Fill in the gaps.
Anode voltage is +5V, cathode V is +3V. The diode is _____. Anode voltage is -5V, cathode V is -3V. The diode is _____.

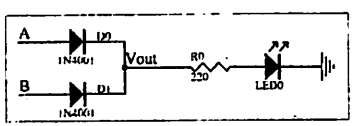
A. ON, ON B. OFF,OFF C. ON, OFF D. OFF, ON E. float, float

Answer: If anode voltage of diode is +5V and it is cathode voltage is +3V it is forward biased so the diode is ON. But if voltage on anode of diode is -5V and on cathode is -3V the diode is reverse biased because voltage on anode is less than voltage on cathode. So the diode is OFF.

156. Forward bias means that for diode
A. anode voltage is more positive than its cathode one
B. anode voltage is equal to or is more negative than its cathode one
C. anode voltage is positive D. anode voltage is negative
E. anode voltage is more negative than its cathode one

Answer: By definition forward bias means that for diode anode voltage is more positive than it is cathode one.

157. For the circuit below if V_A=5V V_B=0V D_0 is _____, D_1 is _____, and LED_0 is_____.
A. ON, OFF, ON B. ON, ON, ON C. OFF, OFF, OFF
D. OFF, ON, ON E. ON, ON, OFF

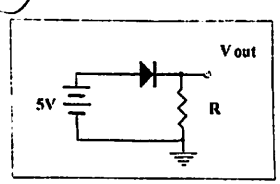


For the circuit below if V_A=5 V_B = 0 . D_0 will be forward biased and D_1 will be reverse-biased. So the +5v voltage will go through the D_0 and V_{out} will be 4.3 V. Since the V_{out} is connected to anode of LED_0 and it is cathode is on ground the led will be ON.

158. Calculate current through typical red LED if resistor for its limitation is equal to 330 Ω. Anode voltage of LED is 5V.
A. 10 mA B. 15 mA C. 20 mA D. 25 mA E. 30 mA

Since the typical voltage on led is 1.7 V the voltage on the resistor will be 5-1.7=3.3V So the current on it will be I=V/R = 3.3/330 = 10 mA.

159. For the circuit below define current through diode if R=2kΩ



A. 5 mA
B. 4.5 mA
C. 4.3 mA
D. 2.15 mA
E. 0.86 mA

By the scheme we can see that current will be equal everywhere so we can find current on resistor. I=V/R Voltage on resistor equal to 5-0.7=4.3 V since voltage gain of diode. So current is I=V/R=4.3/2=2.15 mA.

160. Fill in the gaps in the text: to turn on an NPN transistor, a _____ voltage is applied to the _____. When transistor is turned on, its collector-to-emitter becomes a _____
A. negative, base, short B. positive, base, short C. negative, emitter, open,
D. positive, emitter, short E. positive, emitter, open

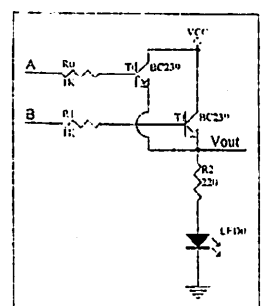
By the definition to turn on NPN transistor a positive voltage must be applied to the base. Then transistor will be ON and short circuit will appear.

161. Bipolar transistor has:
A. 1 p-n-junction B. 2 p-n-junctions C. 3 p-n-junctions
D. 1, 2, or 3 p-n-junctions E. any number of p-n-junctions

By definition Bipolar transistor has 2 p-n junctions.

162. For the circuit below if V_A=0 V_B=0 transistor T_0 is____, transistor T_1 is_____, LED_0 is____.

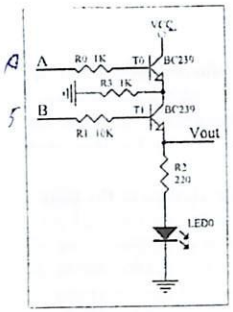
A. ON, ON, ON B. ON, ON, OFF C. OFF,ON, OFF
D. OFF, OFF, ON E. OFF, OFF, OFF



Since V_A=0 (base) and emitter voltage of T_0 is 0. Since V_B=0(base) and emitter voltage of T_1=0 and no voltage passage LED_0 is OFF.

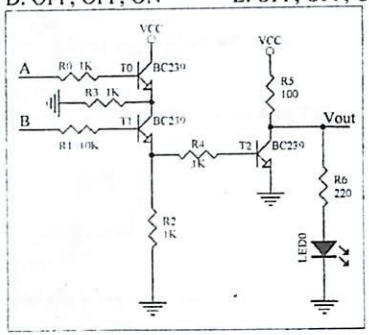
163. For the circuit below if V_A=0 V_B=5V transistor T_0 is____, transistor T_1 is_____, LED_0 is____.
A. ON, ON, ON B. ON, ON, OFF C. OFF,ON, OFF
D. OFF, OFF, ON E. OFF, OFF, OFF

Since V_A=0 (base) and emitter voltage of T_0 is 0. Since V_B=5(base) and emitter voltage of T_1=5 and no voltage passage LED_0 is OFF.



164. For the circuit below if V_A=5V V_B=0 transistor T_0 is____, transistor T_1 is_____, transistorT_2 is____.

A. ON, ON, ON B. ON, OFF, OFF C. OFF,ON, OFF
D. OFF, OFF, ON E. OFF, OFF, OFF



Since V_A=5 (base) and emitter voltage of T_0 is 5. Since V_B=0 (base) and emitter voltage of T_1=0 and voltage on base T_2=0.

165. What is the result of the following BCD addition?

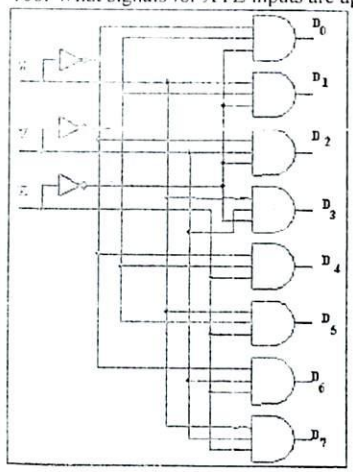
0011 0010 1001 0101
\+ 0111 0000 0110

A. 0011 1001 1001 1011 B. 0100 0000 0000 0001 C. 0011 1001 1001 0001
D. 0100 0000 0000 1011 E. 0011 0000 0000 1011

0011 0010 1001 1011
\+ 0111 0000 0110

0100 0000 0000 0001

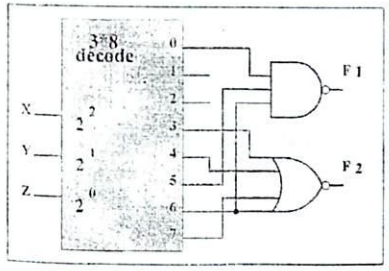
166. What signals for XYZ inputs are applied if active output is D_0?



A. 0, 0, 0
B. 0, 1, 1
C. 1, 0, 0
D. 0, 1, 0
E. 0, 0, 1

D_0 AND gate can receive only inverted function of X Y Z inputs .So it will be 0 0 0 .

167. What function F_1 is implemented with a decoder and external gate?



A. 0
B. 1
C. XY
D. X'Y'
E. XYZ'

Function is (X'Y'Z')(XYZ')(XY'Z)= X'X Y'Y ZZ'= 0* Y'YZZ'=0

168. What statement is correct?

A. A decoder can be realized on the basis of OR gates.
B. A decoder can be used as a MUX.
C. A decoder can be used as a data selector.
D. A 3-to-8 line decoder can be used for a binary-to-BCD conversion.
E. A 3 to-8 line decoder can be used for a binary-to-octal conversion.

Correct answer — E: 3-to-8 line decoder can be used for a binary-to-octal conversion. Since this decoder accepts 3bit binary number (0..7) and outputs 7 unique numbers, it can obviously be used for this conversion.

169. Fill in the gaps.

If we use NAND gates for decoder the outputs will be active-____. It means that only one output will be _____ at the moment, others will be _____.

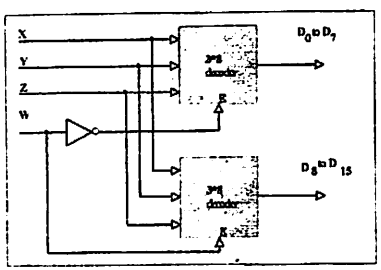
A. HIGH, HIGH, LOW B. HIGH, LOW, HIGH C. LOW, HIGH, HIGH
D. LOW, LOW, HIGH E. all answers are wrong

Correct answer — D: LOW, LOW, HIGH
If we use NAND gates for decoder then the outputs will be Active-LOW (because of NAND). Active-LOW output of a decoder means that we obtain only one "0" (true), all other signals are "1" (false).

170. A group of flip-flops sensitive to pulse transition is called a_____
A. ripple counter B. transceiver C. synchronous counter D. latch E. register

According to definition, a group of flip-flops sensitive to pulse transition is called a register.

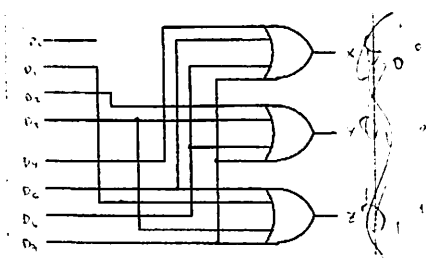
171. What input signals must be applied to WXYZ for the circuit below if D_8 is generated as output?



A. 0110
B. 0111
C. 1000
D. 1001
E. 1010

Correct answer — C: 1000
Since we have to obtain D8 we disable first decoder (W=1) and then obtain very first line of the second one by placing zeros to the rest inputs (X=Y=Z=0).

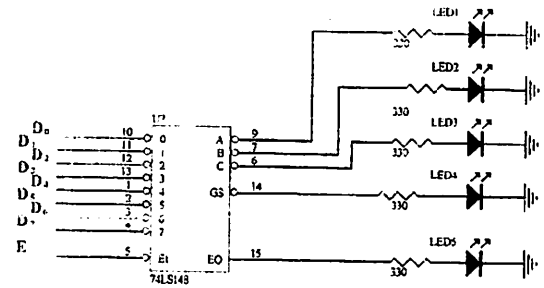
172. If D_1 is active input outputs XYZ will be _____



A.111
B. 100
C.101
D.011
E. 001

Correct answer — E: 001
Since all inputs except D1 are not active, X and Y are equal to 0. Z is equal to 1 because it has D1 as one of its inputs.

173. For the circuit below if EI=5V, D_1=0, D_5=0 the state of L_1 to L_5 will be.



A. ON,ON,ON,ON,ON B. OFF,OFF,OFF,ON,ON
C. ON,ON,ON,OFF,OFF D. OFF,OFF, ON,ON,ON,
E. OFF, ON,ON,ON, OFF

Correct answer — A: ON,ON,ON,ON,ON
Since chip is disabled (HIGH placed to active-LOW Enable Input of octal-to-binary priority encoder), all outputs are set on (inactive state).

174. How many bits does it need to encode the information according to three different features? The first feature may be of three types, the second and the third – of six types.
A.4 B.6 C.8 D.10 E.12

Correct answer — C: 8
We have an instance of information that contains 3 coded "features". Three different states of the first feature we can define by a 2-bit number. Six types, hence, can be defined by 3-bit number. Now simply count: 2 + 3 + 3.

175 What is the 5-digit hex address of the 400th memory location? (First memory location is 00000).
A. 0018C B. 0019F C. 0018F D. 0018D E. 0019C

Correct answer — C: 0018F
400th memory location is actually 399th, because we start counting from 0. Hence $(399)_{10}$ = $(18F)_{16}$

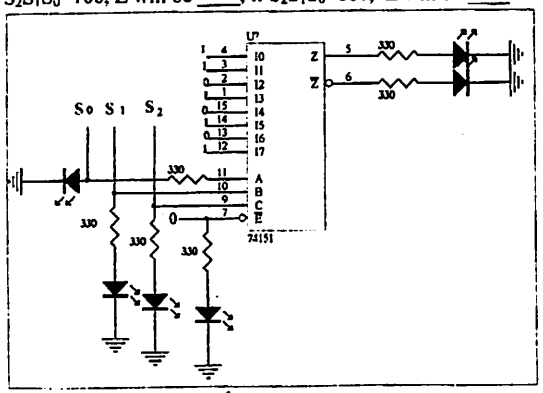
176. 4AH number is transmitted in serial mode, least significant digit first. Frequency of transmission is 4 kHz. What is the state of the serial line 0.6, 0.8, 1.6 ms into the transmission?
A. 0,1,0 B. 1,0,0 C. 1,0,1 D. 0,1,1 E. 1,1,1

4 digits are sent during 1ms, hence each digit "lasts" for 0.25ms. Number 4AH in binary is 0100 1010. Since LSB is sent first, at 0.6ms 3rd digit of A is sending (0), at 0.8ms — 4th (1), at 1.6ms — 3rd digit of 4 (1).

177. If 100 memory locations are used for data storage starting at location 000C8H what is the location of the last data item?
A. 0012CH B. 0013EH C. 0013BH D. 0012FH E. 0012BH

Correct answer — E: 0012BH
Task is simple, because we need to add 99 units to the starting address (remember that we count from it). Converting 99 to hex (63) and adding the result to starting position (C8) we obtain 12B.

178. For the circuit below if selection lines $S_2S_1S_0$=011 the output Z will be ____, if $S_2S_1S_0$=100, Z will be ____, if $S_2S_1S_0$=001, Z will be ____.



A. 1,1,0 B. 0,1,1 C. 1,1,1 D. 0,1,0 E.1,0,1

Correct answer — E: 1, 0, 1
Remind working principles of a multiplexer: convert selection lines number to decimal and add 1 to obtain number of line to be selected.

179. The main property of the p-n-junction is ability.....
A. to increase the potential. B. to decrease the potential.
C. to increase the current. D. to decrease the current.
E. to allow the current flow actually only in one direction.

Correct answer — E: The main property of the p-n-junction is ability to allow the current flow actually only in one direction.

Remind the corresponding definition. Hint: do you remember how does simple diode work? Current can flow only in one direction (current flowing in the opposite direction is very small and hence negligible). Diode is an example of a simple p-n-junction.

180. Determine the period of a clock waveform, whose frequency is 500 kHz.
A. 5μs B. 2μs C. 2ms D. 5ms E. 2ns
Correct answer — B: 2μs

Period (T) is equal to the reciprocal of the frequency.

181. Determine the radix r for the case: $(144)_{10}=(100)_r$.
A.9 B.11 C.12 D.13 E. 14

Correct answer — C: 12
Hint: use you intuition and count ability :)

144	**:**	**12**	**=**	**12**	**+**	**0**
12	**:**	**12**	**=**	**1**	**+**	**0**
1	**:**	**12**	**=**	**0**	**+**	**1**

$144=1*r^2+0*r+0$
$144=r^2$
r 12
r -12
since r can not be negative r=12.(C)

182. F(A,B,C)= $\sum(0,1,6,7)$. Define simplified expression for the function.
A. A⊕B B. A⊙B C. B⊕C D. B⊙C E. AB

Correct answer — B: A⊙B
Lets simplify given sum of products: A'B'C' + A'B'C + ABC' + ABC = A'B'(C' + C) + AB(C' + C) = /* hint: C' + C = 1 */ = A'B' + AB. Hence, given sum of products is pure XNOR of A and B.

183. The function F(A,B,C,D)=A'BC'D'+A'BCD'+ABD+AB'D is reduced to AD+A'B. What are don't-care conditions?
A.A'BC B.ACD C.A'BD D.ABD E.ABC

Correct answer — C: A'BD
Refer to the table below:

	C'	C'	C	C	
A'					B'
A'	1	X	X	1	B
A		1	1		B
A		1	1		B'
	D'	D	D	D'	

184. A and B outputs of Johnson shift counter are connected to an AND gate and standard sequence begins at t=0 ms. Period of whole sequence is equal to 8 ms. Define the period of time when output of AND gate is HIGH.
A. from 1 to 2 ms B. from 1 to 4 ms C. from 2 to 3 ms D. from 0 to 5 ms E. from 3 to 5 ms

Correct answer – B: from 1 to 4 ms
Because A and B are not HIGH simultaneously only between 0 and 1 ms and 4 to 8 ms

185. The second strip to obtain resistance 560 Ω must be
A. blue B. Green C. Brown D. Yellow E. red

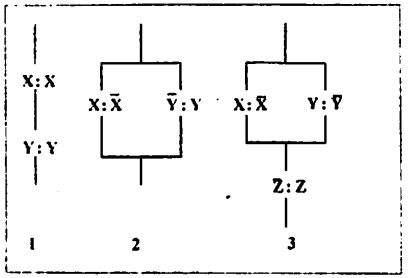
Correct answer — A: blue
The second strip have to be blue to obtain 560 Ω. Refer to resistances table.

186. We have got the simplified expression of the function F(A,B,C,D)=AB'+ACD'. Express the function as sum of minterms.
A. ∑(2,3,5,6,7,13,15) B. ∑(1,3,11,12,14,15) C. ∑(1,2,7,8,9,13,15)
D. ∑(8,9,10,11,14) E. ∑(0,1,2,3,7,9,11,13)

	C'	C'	C	C	
A'	0	1	3	2	B'
A'	4	5	7	6	B
A	12	13	15	14	B
A	8	9	11	10	B'
	D'	D	D	D'	

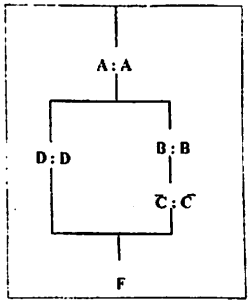
Shaded area gives us answer of this question: 8, 9, 10, 11, 14(D)

187. In the scheme below __ channel is used, in the second - __ channel, in the third - _____ channel. A. P, N, N B.P,N,P C. N,P,N D.N,P,P E. P,P,N



The answer is N,P,P(D)

188. Find Boolean function F that corresponds to the closed paths through the given network below
A.A(D+BC`) B. A+(BC`D) C.A(D`+BC`) D.A`(D+BC`) E.A(B`C+D)



B and C` is connected in series and their result is connected in parallel with D this gives us
B.C`+D and this expression is connected in series with A
So the answer is A(D+BC`) . (A)

189. For applying AND-OR-INVERT implementation function must be
A. normalized B. simplified C. in sum-of-products form
D. in product-of-sums form E. in complement form

C (according to definition)

190. Determine the radix r for the case: $(87)_{10}=(153)_r$. A.9 B.8 C.7 D.6 E. 5

$87=1*r^2+5*r+3$
$0=r^2+5*r-84$
$r \quad 12$
$r \quad -7$
since r can not be negative r=7.(C)

191. What device is used for troubleshooting?
A. transistor B.IC C. logic probe D.logic pulse E. answer C and D are both correct

E (according to definition)

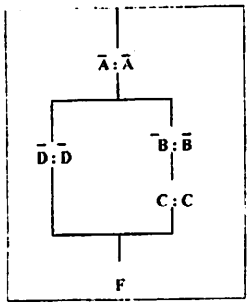
192. What is totem-pole arrangement?
A. 2 transistors B. 3 transistors C. 2 transistors and diode
D. 2 transistors and diode between them E. 2 transistors and 2 diodes

D (according to definition)

193. Johnson shift counter produces _____ different signals simultaneously.
A.4 B.6 C.8 D.10 E.12

C (according to definition)

194. Find Boolean function F that corresponds to the closed paths through the given network below
A.A(D+BC`) B. A+(BC`D) C.A(D`+BC`) D.A`(D+BC`) E.A`(B`C+D`)



B' and C is connected in series and their result is connected in parallel with D' this gives us
BC'+D and this expression is connected in series with A'. So the answer is A'(D'+B'C)
.(E)

195. Expression of the function F=∑(0, 3, 5, 7) in product of maxterms form is:

A. F=∏ (1, 2, 3, 4) B. F=∏(4, 5, 6, 7) C. F=∏(1, 2, 6, 7)
D. F=∏(1, 2, 4, 5) E. F=∏(1, 2, 4, 6)

Function is given sum of minterms, since while expressing function in sum of minterms we use ones and maxterms we use zeros, to convert from sum of minterms to product of maxtrems we just use those numbers which are not in the given set. They are 1,2,4,,6.(E)

196. . What is typical voltage drop for red LED?
A. 0.5V B. 1V C. 1.5V D. 1.7V E. 2V

D (according to definition)

197. Interpret this truth table in negative logic:
A.AND B. NAND C.OR D.NOR E.XOR

x	y	F
L	L	L
L	H	L
H	L	L
H	H	H

To convert from positive logic to negative logic we replace HIGH with LOW and LOW with HIGH. Our table becomes:

X	Y	F
H	H	H
H	L	H
L	H	H
L	L	L

This truth table of OR (C)

198. For what function its dual is equal to its complement?

A. XNOR B. OR C. NOR D.AND E. NAND
A (according to definition)

199. Binary conversion of decimal 12 is _____, the coding it in BCD is _____
A. 1101, 00010011 B. 1101, 1100 C. 1101, 1111 D. 1100, 01101100
E. 1100, 00010010

number	mod2
12	0
6	0
3	1
1	1

So the binary code of 12 is 1100. BCD code of 12 is 0001 00010.

200. Result of multiplication of $(13)_6$ by $(42)_6$ is equal to
A.276 B.402 C. 1030 D. 1002 E. 376
The answer is C.

13
× 42
210
+ 42
1030

1.4 R = 560 Ωm
↓
blue

1.5 . R = 9600 Ωm
↓↓↓
white, blue, Red

$96 \cdot 10^2$

2.5 120 Ωm
↓
Red

2.6 $(XY)' = (X + Y')$ → wrong

ANSWER KEYS.

1	A	51	B	101	B	151	D
2	E	52	E	102	A	152	B
3	A	53	A	103	A	153	B
4	A	54	C	104	C	154	B
5	A	55	E	105	E	155	C
6	A	56	A	106	B	156	A
7	E	57	B	107	C	157	A
8	B	58	E	108	E	158	A
9	A	59	C	109	C	159	D
10	E	60	C	110	D	160	B
11	C	61	B	111	E	161	B
12	A	62	C	112	E	162	E
13	E	63	E	113	E	163	C
14	A	64	A	114	E	164	B
15	C	65	A	115	E	165	B
16	B	66	E	116	A	166	A
17	A	67	E	117	D	167	B
18	A	68	C	118	C	168	E
19	A	69	E	119	C	169	D
20	D	70	A	120	E	170	E
21	B	71	B	121	B	171	C
22	A	72	C	122	C	172	E
23	C	73	E	123	C	173	A
24	B	74	C	124	B	174	C
25	A	75	C	125	B	175	C
26	B	76	E	126	B	176	D
27	D	77	D	127	C	177	E
28	B	78	D	128	C	178	E
29	D	79	C	129	C	179	E
30	E	80	D	130	C	180	B
31	B	81	B	131	B	181	C
32	A	82	E	132	C	182	B
33	E	83	A	133	B	183	C
34	C	84	C	134	B	184	B
35	E	85	E	135	B	185	A
36	C	86	A	136	C	186	D
37	B	87	E	137	C	187	D
38	A	88	C	138	E	188	A
39	D	89	D	139	A	189	C
40	B	90	D	140	E	190	C
41	D	91	C	141	A	191	E
42	D	92	C	142	A	192	D
43	E	93	D	143	D	193	C
44	E	94	A	144	B	194	E
45	C	95	B	145	E	195	E
46	C	96	D	146	C	196	D
47	A	97	E	147	D	197	C
48	D	98	D	148	C	198	A
49	B	99	B	149	C	199	E
50	B	100	A	150	A	200	C

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