SULEYMAN DEMIREL UNIVERSITY
ENGINEERING FACULTY

CIRCUIT TECHNOLOGIES
LABORATORY WORKS
DESCRIPTIONS AND TEST EXAMPLES

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CONTENTS

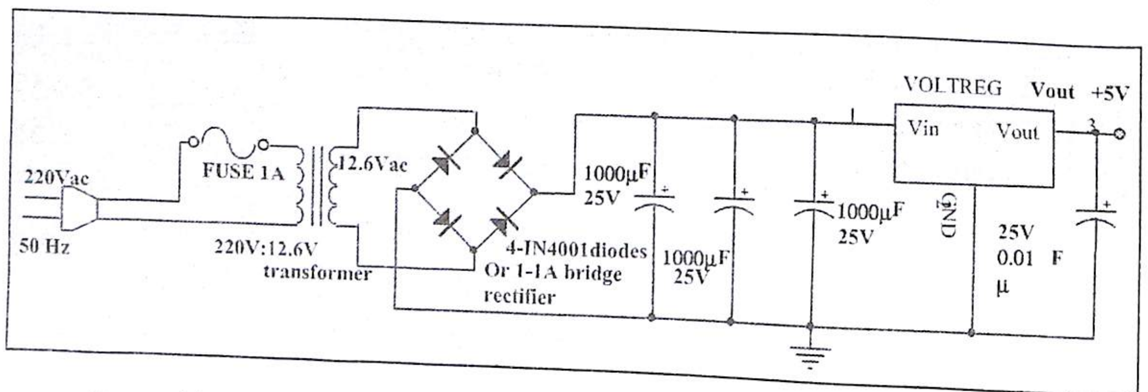
PREFACE

Laboratory works on the course "CIRCUIT TECHNOLOGIES" are worked out for provision of more deep understanding of basic digital circuits' operation. They cover such circuits as logic gates, code converters, decoders, encoders, multiplexers, demultiplexres, adders, flip-flops. They are used to improve students' investigation skills.

In process of lab works' performance students must improve their skills of analysis and synthesis of digital circuits, investigate modes of their operation. The important part of the student's work is Scheme Design System application for the schemes' preparation. Doing the lab works students must understand the functionality of the circuits deeply and to be sure that it operates in full correspondence with its theoretical description. Lab works can be very helpful to provide hands-on reinforcement of the theoretical knowledge.

Performance of lab works provides presence and development the students' skills to mount electronic schemes, to treat with measuring instruments and evaluate their readings correctly. The students must obtain skills to define the function of chips and how to treat with them. Throughout the labs, the standard integrated circuits are used to provide students' proficiency at using the terminology and data sheets of the ICs.

To perform lab works the following power supply scheme is used:



It provides presence of 5V dc as output voltage at each working place. Such value of voltage is not dangerous for the human life, so laboratory installation has full correspondence to safety rules.

PRELIMINARIES 1.

RESISTORS' COLORED CODES.

Codes may have a view of colored strips or dots. Each color has got its own definite meaning (see table). Strips put to one of the resistor's terminal and are situated from left to right. If the size of the resistor doesn't allow us to place strips in such a way the first strip of each resistor is made wider than others. Resistors of low accuracy (0.1%-10%) are marked with 5 colored strips. The first three are resistance in Ohms, the forth – multiplier, the fifth – accuracy. If resistors are marked with 4 colored strips the first two are resistance in Ohms, the third – multiplier, the forth -accuracy. If a resistor has got 3 colored strips it means that the first two strips are shown value of resistance in Ohms, the third one is multiplier.

Strip's color	Nominal resistance, Ohm			Multiplier	Tolerance, %
	First strip	Second strip	Third strip	Forth strip	Fifth strip
Silver	-	-	-	0.01	±10
Golden	-	-	-	0.1	±5
Black	-	0	-	1	-
Brown	1	1	1	10	±1
Red	2	2	2	10^2	±2
Orange	3	3	3	10^3	-
Yellow	4	4	4	10^4	-
Green	5	5	5	10^5	±0.5
Blue	6	6	6	10^6	±0.25
Violet	7	7	7	10^7	±0.1
Gray	8	8	8	10^8	-
White	9	9	9	10^9	-

1,000 Ω

br bl orang

PRELIMINARIES 2.

MEASUREMENTS with DIGITAL MULTIMETER.

Digital multimeter is a multifunctional instrument. It can measure resistance capacitance, DC and AC voltage, DC and AC current, short-circuit. It can help us to define transistor's base, emitter and collector, anode and cathode for diode.

Process of measurement.
Before the work it needs to check if the instrument ready to work. For this purpose in the mode "measurement of resistance" it needs to connect test leads (range of measurement is 200 Ω). The sound signal will appear to inform us about short-circuit. It means that the instrument is suitable for measurement. This mode is used for searching short-circuit somewhere in the electric circuit. In other positions of the pointer (not "measurement of resistance") we can see 0 on the display without contact between the leads.

1. Measurement of resistance.

Set the FUNCTION switch to the position "measurement of resistance" and connect the test leads across the resistor under measurement. Connect the BLACK test lead to the COM jack and the RED test lead to the V/Ω jack. After checking define range of measurement. For example, 200 Ω. If resistance of resistor under measurement is higher, the readings will be 1. Change the range. If resistance under measurement is over this range, we have got its value on the display.

2. Measurement of DC voltage.

Set the FUNCTION switch to the position "measurement of DC voltage" and connect the test leads across the source or load under measurement. Connect the BLACK test lead to the COM jack and the RED test lead to the V/Ω jack. After checking define range of measurement. Range for DCV-200mV-1000V. For DCV: if polarity is wrong, indications will be with sigh "-". About correctness of measurement range we can judge comparing measuring parameter and chosen range. If measuring parameter is over the lower measuring range, you should switch the FUNCTION switch to it to increase measurement accuracy. If measuring parameter is out of the range there is 1 on the display. In case of measurement of the same value in different ranges the accuracy of measurement will be different. For example, if V=1.5V: range 2V- the result is 1.505 V(three digits after decimal point); range 20V-the result is 1.51V(two digits after decimal point); range 200V-01.5V (one digit after decimal point). To increase accuracy it needs to choose the range, which corresponds to measuring parameter.

3. Definition of p-n-junction resistance.

In spite of the fact that it is resistance, we can't use position of the FUNCTION switch "measurement of resistance". We will see 1 on the display in this case. We must use for the switch a special position, where convention of the diode is situated. Test leads are in the position for voltage measurement. We touch pins of the diode by test leads. If we have reverse bias, we can see 1 on the display. If it is forward bias, we can see some definite value on the display. It is the diode's resistance and it is definition of the diode's anode and cathode. RED test lead in this case is connected with anode. If the diode is LED one, it can light.

LABORATORY WORK # 1.

DIODE APPLICATIONS

Aims: investigate properties of diodes and LEDs, get skills of the scheme mounting. Compare experimental results with theoretical foundations about diodes.

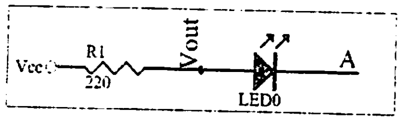
PREPARATION TO LAB WORK.

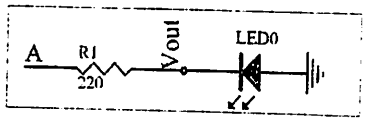
1 Learn the information about diodes and LEDs.
2 Show semiconductor diode i-v-characteristic.
3 Consider experiments' schemes and draw them with application of Scheme Design System. Fill in the tables theoretically.
4 Answer the questions below in written form.
- 4.1 What is a semiconductor diode?
- 4.2 What is diode's forward/reverse bias?
- 4.3 What is diode's cathode/anode?
- 4.4 How can you define cathode and anode for real diode?
- 4.5 Explain a semiconductor diode's behavior according to its i-v-characteristic.
- 4.6 What is LED?
- 4.7 Explain how to define the value of resistance for any resistor.
- 4.8 Explain how to measure voltage with multimeter.

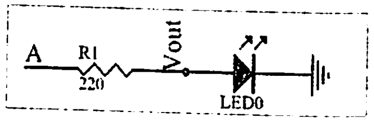
LAB WORK PERFORMANCE.

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount the schemes of experiment 1A on the breadboard and perform them.
5. Make a conclusion about functionality of the schemes. Compare your results with theoretical ones.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Repeat steps 4 to 6 for experiment 1B.
8. Be ready to answer your instructor's questions in process of work.
9. Complete your work, dismount your schemes, clean your working place.
10. Answer your instructor's final questions, obtain your mark.
11. Ask your instructor's permission to leave.

Experiment 1A. Realize the following circuit on a breadboard. Connecting A, and B inputs t either GND or VCC based on the following table, fill in the blanks. Write ON or OFF fo LEDs.





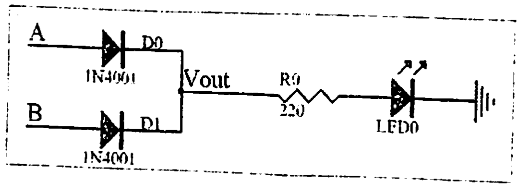


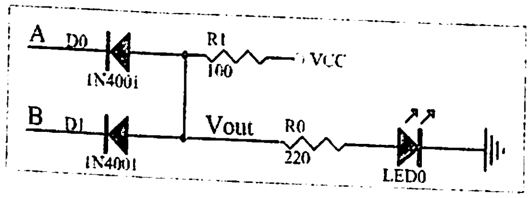
	INPUT	OUTPUT	
	A	LED 0 ON/OFF	Vout (V)
1	5V	OFF	4.76
2	0V	ON	[illegible]

	INPUT	OUTPUT	
	A	LED 0 ON/OFF	Vout (V)
1	5V		4.76
2	0V		0

	INPUT	OUTPUT	
	A	LED 0 ON/OFF	Vout (V)
1	5V		[illegible]
2	0V	[illegible]	0

Experiment 1B. Do the similar things for the following circuits.



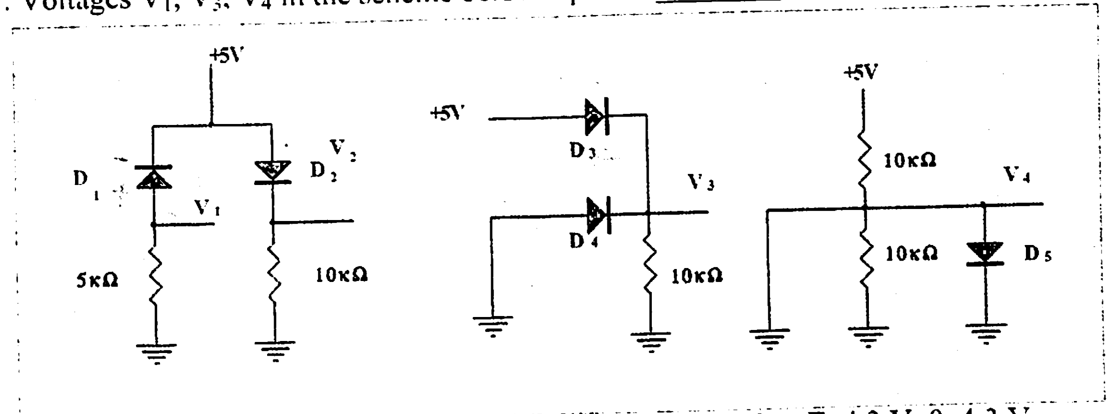


	INPUTS		OUTPUTS	
	A	B	LED0	Vout (V)
1	0V	0V		[illegible]
2	0V	5V		[illegible]
3	5V	0V		[illegible]
4	5V	5V		[illegible]

	INPUTS		OUTPUTS	
	A	B	LED0	Vout (V)
1	0V	0V	on	1.99
2	0V	5V	on	[illegible]
3	5V	0V	on	[illegible]
4	5V	5V	on	[illegible]

TEST QUESTIONS

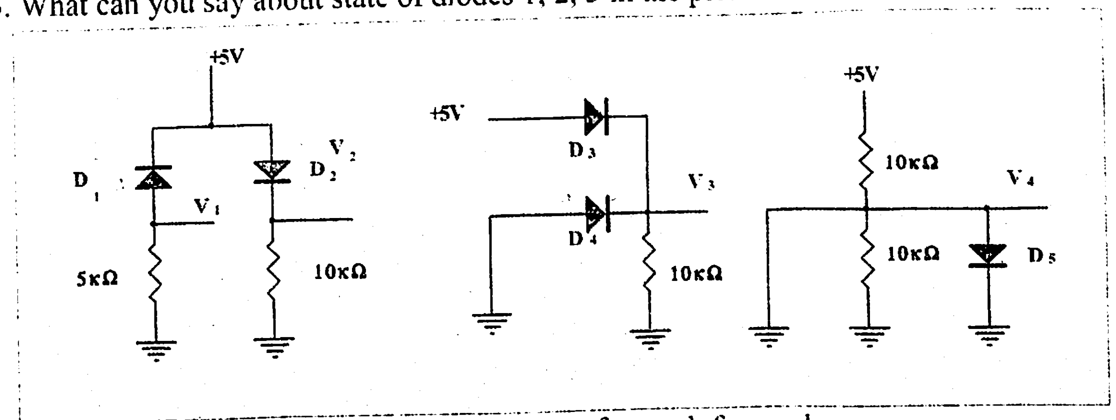
1. Voltages V_1, V_3, V_4 in the scheme below equal to ________ respectively.



A. 4.3 V, 0, 0 B. 0, 4.3V, 0 C. 4.3 V, 4.3 V, 0 D. 0, 0, 0 E. 4.3 V, 0, 4.3 V

2. How many states has the switch got?
A. 1 B. 2 C. 3 D. 4 E. 5

3. What can you say about state of diodes 1, 2, 3 in the picture?



A. reverse, forward, reverse B. reverse, forward, forward
C. forward, reverse, forward D. Reverse, reverse, forward
E. forward, forward, reverse

4. The second strip to obtain resistance 560 Ω must be
A. blue B. Green C. Brown D. Yellow E. red

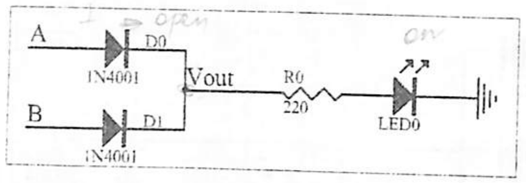
5. Value of resistance is 9.6 kΩ. It means that the first three strips on the resistance case (in whole the case has got 4 strips) are:
A. white, blue, red B. gray, brown, black C. Black, brown, green
D. brown, black, brown E. brown, black, red

6. Analyze the information. Fill in the gaps.
Anode voltage is +5V, cathode V is +3V. The diode is ______. Anode voltage is -5V, cathode V is -3V. The diode is ______.
A. ON, ON B. OFF,OFF C. ON, OFF D. OFF, ON E. all answers are wrong

7. Forward bias means that for diode
A. anode voltage is more positive than its cathode one
B. anode voltage is equal to or is more negative than its cathode one
C. anode voltage is positive D. anode voltage is negative E. all answers are wrong

8. For the circuit below if V_A=5V V_B=0V D_0 is ______, D_1 is ______, and LED_0 is________.

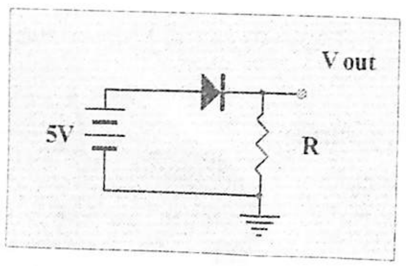
A. open, closed, ON B. open, open, ON C. closed, closed, OFF
D. closed, open, ON E. open, open, OFF



9. Calculate current through typical red LED if resistor for its limitation is equal to 330 Ω. Anode voltage of LED is 5V.

A. 10 mA B. 15 mA C. 20 mA D. 25 mA E. 30 mA

10. For the circuit below define current through diode if R=2kΩ



A. 5 m
B. 4.5 m
C. 4.3 m
D. 2.15 m
E. 0.86 m

LABORATORY WORK # 2.

REALIZATION OF LOGIC GATES WITH TRANSISTORS.

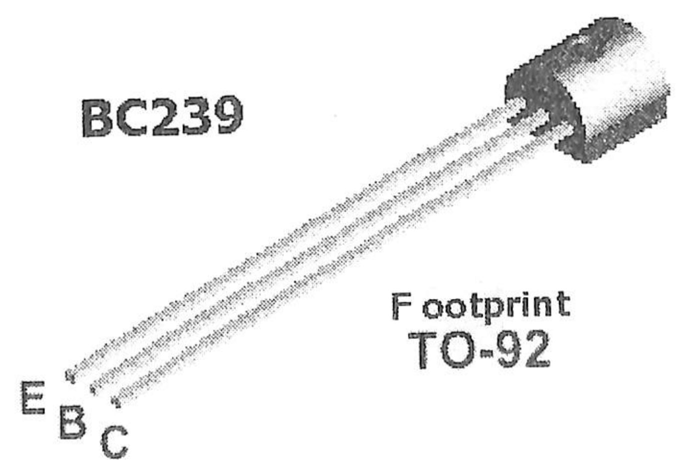
Aims: define what logic gates are realized schematically, learn the gates' properties. Compare experimental results with theoretical foundations about logic gates.
Improve skills of the schemes' preparation.

PREPARATION TO LAB WORK.

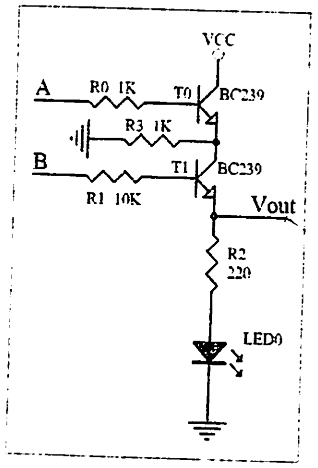
1 Learn the information about transistors.
2 Show bipolar transistor's characteristics.
3 Consider experiments' schemes and draw them with application of Scheme Design System. Analyze what gates are realized on the schemes' basis. Fill in the tables theoretically.
4 Answer the questions below in written form.
 4.1 What is a bipolar transistor?
 4.2 What are names of a bipolar transistor's electrodes?
 4.3 How to define situation of a bipolar transistor's electrodes?
 4.4 What are conditions to have a bipolar transistor ON(OFF)?
 4.5 What types of bipolar transistors do you know?
 4.6 What are typical silicon transistor's parameters?
 4.7 What modes of a bipolar transistor's operation do you know?

LAB WORK PERFORMANCE.

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount the first scheme of experiment 2 on the breadboard and perform it.
5. Make a conclusion about functionality of the scheme. Compare your results with theoretical ones.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Repeat steps 4 to 6 for the second and third schemes of experiment 2.
8. Be ready to answer your instructor's questions in process of work.
9. Complete your work, dismount your schemes, clean your working place.
10. Answer your instructor's final questions, obtain your mark.
11. Ask your instructor's permission to leave.

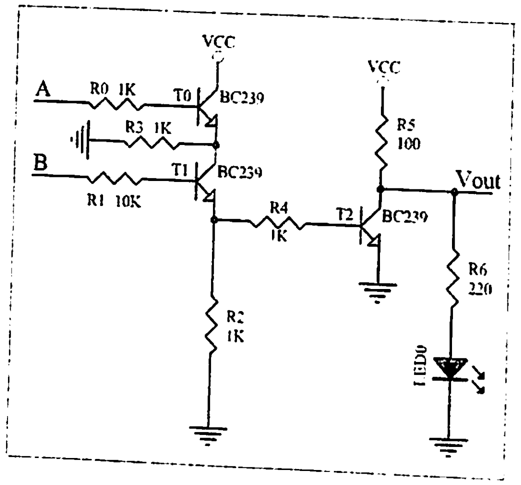


Experiment 2. Realize the following circuit on a breadboard. Connecting A, and B inputs to either GND or VCC based on the following table, fill in the blanks. Write ON or OFF for LEDs.



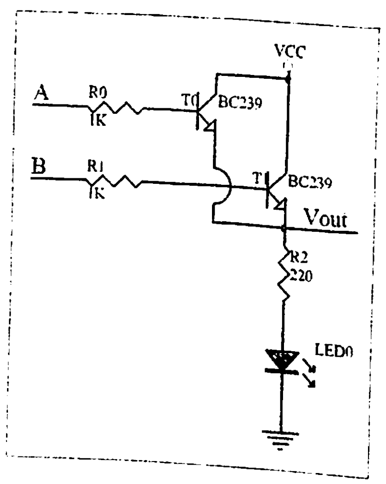
	INPUTS		OUTPUTS	
	A	B	LED	Vout
1	0V	0V	off	0,41
2	0V	5V	off	0,33
3	5V	0V	off	0,33
4	5V	5V	on	[illegible]

This is ....and.... Gate



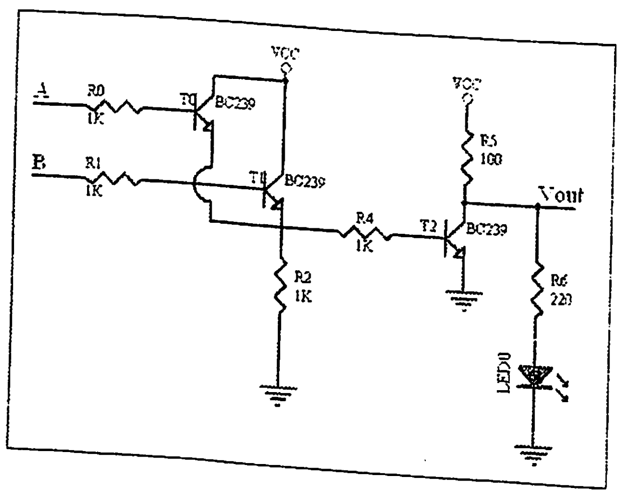
	INPUTS		OUTPUTS	
	A	B	LED	Vout
1	0V	0V	on	
2	0V	5V	off	
3	5V	0V	off	
4	5V	5V	off	

This is a ....nand.... Gate



	INPUTS		OUTPUTS	
	A	B	LED	Vout
1	0V	0V	off	
2	0V	5V	off	
3	5V	0V	off	
4	5V	5V	on	

This is ....or.... Gate



	INPUTS		OUTPUTS	
	A	B	LED	Vout
1	0V	0V	on	
2	0V	5V	on	
3	5V	0V	off	
4	5V	5V	off	

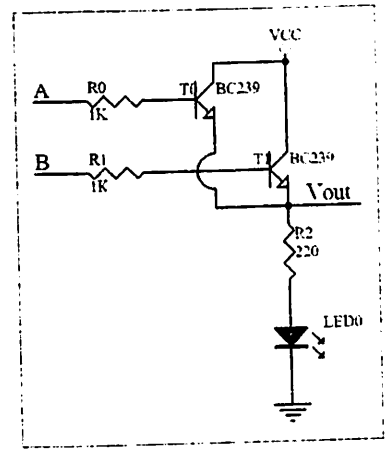
This is a ....[illegible].... Gate

TEST QUESTIONS

1.For the circuit below if V_A=0 V_B=0 transistor T_0 is____, transistor T_1 is_____, LED_0 is____.

A. ON, ON, ON B. ON, ON. OFF C. OFF,ON, OFF

D. OFF, OFF, ON E. OFF, OFF, OFF



2.Fill in the gaps in the text: to turn on an NPN transistor, a ______ voltage is applied to the ______. When transistor is turned on, its collector-to-emitter becomes a _____.

A. negative, base, short B. positive. base, short C. negative, emitter, open

D. positive, emitter, short E. positive, emitter, open

3. How many states has the switch got?

A. 1 B. 2 C. 3 D. 4 E. 5

4. Bipolar transistor has:

A. 1 p-n-junction B. 2 p-n-junctions C. 3 p-n-junctions

D.1, or 2, or 3 p-n-junctions E. any number of p-n-junctions

5. The second strip to obtain resistance 120 Ω must be

A. white B. Green C. Brown D. Yellow E. red

6. What statement is wrong?

A. (X+Y)(X+Z)=X+YZ B. X(Y+Z)=XY+XZ C. X+XY=X

D. (XY)′=(X+Y)′ E. X(X+Y)=X

7. The truth table for XOR gate is:

A

X	y	F
0	0	0
0	1	0
1	0	0
1	1	1

B

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

C

x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

D

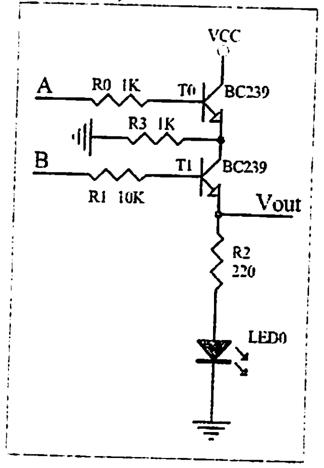
X	y	F
0	0	1
0	1	0
1	0	0
1	1	0

E

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

8. For the circuit below if $V_A=0$ $V_B=5V$ transistor T_0 is____, transistor T_1 is_____, LED_0 is____.

A. ON, ON, ON B. ON, ON, OFF C. OFF,ON, OFF
D. OFF, OFF, ON E. OFF, OFF, OFF



9. The truth table for NAND gate is:

A

X	y	F
0	0	0
0	1	0
1	0	0
1	1	1

B

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

C

X	y	F
0	0	1
0	1	1
1	0	1
1	1	0

D

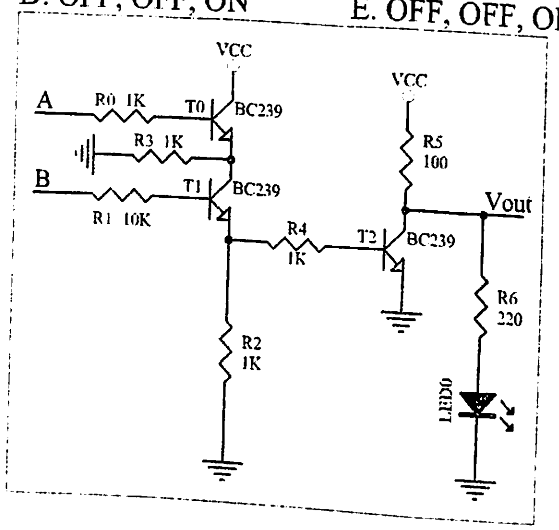
X	y	F
0	0	1
0	1	0
1	0	0
1	1	0

E

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

10. For the circuit below if $V_A=5V$ $V_B=0$ transistor T_0 is____, transistor T_1 is_____, transistorT_2 is____.

A. ON, ON, ON B. ON, OFF, OFF C. OFF,ON, OFF
D. OFF, OFF, ON E. OFF, OFF, OFF



LABORATORY WORK # 3.

LOGIC GATES.

Aims: define what logic gates are realized schematically, learn the gates' properties. Compare experimental results with theoretical foundations about logic gates.

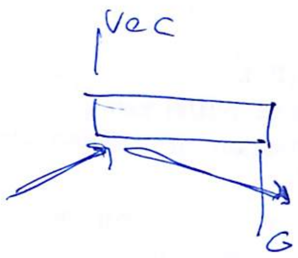
PREPARATION TO LAB WORK.

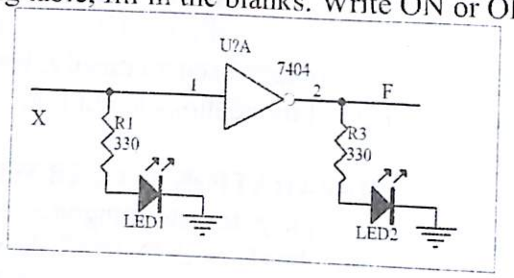
1 Learn the information about logic gates and integrated circuits (IC).
2 Show truth table of AND, OR, NOT, NAND, NOR, XOR, XNOR, buffer gates.
3 Consider experiments' schemes and draw them with application of Scheme Design System. Analyze what gates are realized on the schemes' basis.
4 Design XNOR gate for the experiment 3D on the basis of schemes in experiment 3A, 3B, 3C. Draw the XNOR scheme with application of Scheme Design System.
5 Answer the questions below in written form.
 5.1 What logical operations do you know?
 5.2 Show the algebraic expression of logical operation NOT (AND, OR and so on).
 5.3 How many magnitudes has the logic value got?
 5.4 What is integrated circuit (IC)?
 5.5 What types of IC's do you know?
 5.6 What scales of IC's integration do you know?
 5.7 How many functions of 2 variables do you know?
 5.8 Show the difference between complement and dual functions.
 5.9 What function is called odd (even)?
 5.10 What IC digital logic families do you know?
 5.11 What is positive (negative) logic?
 5.12 What are typical voltage levels for TTL, ECL, CMOS families?
 5.13 What is fan-out, power dissipation, propagation delay, noise margin
 5.14 Compare different IC digital logic families from point of view their typical special characteristics.

LAB WORK PERFORMANCE.

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount the scheme of experiment 3A on the breadboard and perform it.
5. Make a conclusion about functionality of the scheme. Compare your results with theoretical ones.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Repeat steps 4 to 6 for experiment 3B, 3C, 3D.
8. Be ready to answer your instructor's questions in process of work.
9. Complete your work, dismount your schemes, clean your working place.
10. Answer your instructor's final questions, obtain your mark.
11. Ask your instructor's permission to leave.

Experiment 3A. Realize the following circuit on a breadboard. Do not forget to connect 7th of 7404 chip to GND (0V) and 14th pin to VCC (+5V). Connecting X-input to either GND VCC based on the following table, fill in the blanks. Write ON or OFF for LEDs.

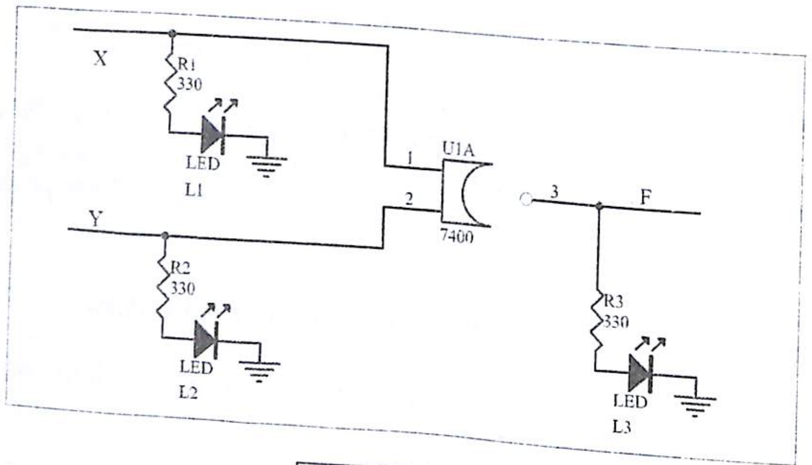




	INPUT	OUTPUT
	X	LED1	LED2
1	0V	off	on
2	5V	on	off

As a result, this truth table belongs to a ....inverse..........

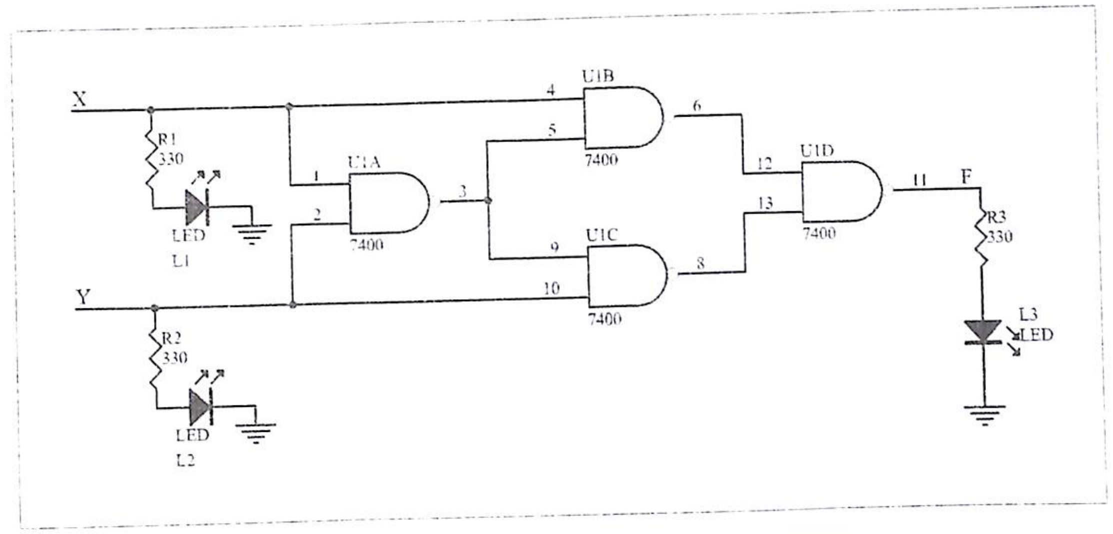
Experiment 3B. Realize the following circuit on a breadboard. Connecting X, and Y inputs either GND or VCC based on the following table, fill in the blanks. Write ON or OFF f LEDs, and a voltage value for F.



	X	Y	INPUTS		OUTPUTS	
			LED1	LED2	LED3	F (V)
1	0V	0V	off	off	on	1,71
2	0V	5V	off	on	on	1,84
3	5V	0V	on	off	off	1,83
4	5V	5V	on	on	off	[illegible]

As a result this truth table belongs to a ....NAND..........

Experiment 3C. Realize the following circuit on a breadboard. Do not forget to connect 7th pin of 7400 chip to GND (0V) and 14th pin to VCC (+5V). Connecting X-input to either GND or VCC based on the following table, fill in the blanks. Write ON or OFF for LEDs.



	X	Y	INPUTS		OUTPUTS	
			LED1	LED2	LED3	F (V)
1	0V	0V	off	off	off	0
2	0V	5V	off	on	on	4,5
3	5V	0V	off	off	on	4,6
4	5V	5V	on	on	off	0

As a result this truth table belongs to a ....xor..........

Experiment 3D. Design XNOR gate on the same scheme basis. Draw the XNOR scheme with application of Scheme Design System.

	X	Y	INPUTS		OUTPUTS	
			LED1	LED2	LED3	F (V)
1	0V	0V	off	off	on	4,61
2	0V	5V	off	on	off	0
3	5V	0V	off	off	off	0
4	5V	5V	on	on	on	4,61

As a result this truth table belongs to a ....xnor..........

TEST QUESTIONS

1. Function # _____ corresponds to function AND of 3 variables.

X	Y	Z	F_1	F_2	F_3	F_4	F_5
0	0	0	0	0	0	0	0
0	0	1	0	0	1	1	0
0	1	0	0	0	1	1	0
0	1	1	1	1	1	1	0
1	0	0	0	1	1	1	0
1	0	1	1	1	1	0	0
1	1	0	1	1	1	0	0
1	1	1	1	1	1	1	1

A. 1 B. 2 C. 3 D. 4 E. 5

2. The truth table for XOR gate is:

A

X	Y	F
0	0	0
0	1	0
1	0	0
1	1	1

B

X	Y	F
0	0	0
0	1	1
1	0	1
1	1	1

C

X	Y	F
0	0	1
0	1	1
1	0	1
1	1	0

D

X	Y	F
0	0	1
0	1	0
1	0	0
1	1	0

E

X	Y	F
0	0	0
0	1	1
1	0	1
1	1	0

3.A small-scale integration (SSI) device contains __________ gates in a single chip.
A. thousands of B. From10 to 1000 C. More than 100
D. From 10 to 100 E. less than 10

4. (XY)′ is algebraic expression of ________ function.
A. XOR B. XNOR C. NOR D. NAND E. AND

5. NOR is dual to A. XOR B. XNOR C. NOR D. NAND E. AND

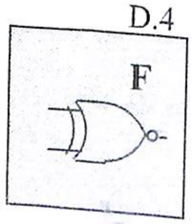
6. OR is complement to A. XOR B. XNOR C. NOR D. NAND E. AND

7. A buffer produces the _____ function.
A. complement B.dual C. transfer D. inhibition E. implication

8. Inverter can have _____ input (s). A. 1 B.2 C. 3 D.4 E. A lot of

9. For the gate below function F is correspondent to column ____.
A.1 B.2 C.3 D.4 E 5

X	Y	1	2	3	4	5
1	1	0	0	1	1	1
1	0	1	0	1	0	0
0	1	1	0	1	0	0
0	0	1	1	0	0	1



10. Duality principle states that every algebraic expression
A. remains valid if the operators and identity elements are changed.
B. remains valid if the operators and identity elements are interchanged.
C. deducible from the postulates of Boolean algebra remains valid if the operators and identity elements are changed.
D. deducible from the postulates of Boolean algebra remains valid if the operators and identity elements are interchanged.
E. deducible from the postulates of Boolean algebra remains valid if the operators are changed.

LABORATORY WORK # 4.

SEVEN-SEGMENT DISPLAYS

Aims: investigate 1-digit and 2-digit seven-segment displays operation, understand the process of code conversion for the device, and make a comparison between 1 and 2 digit seven-segment displays.

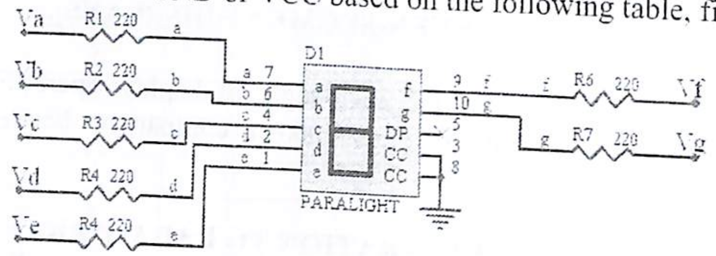
PREPARATION TO LAB WORK.

1 Learn the information about seven-segment displays
2 Consider scheme of experiment 4A and draw it using Scheme Design System.
3 Answer the questions below in written form.
 3.1 What is an order to count pins of a chip?
 3.2 What is a code conversion?
 3.3 What is a BCD-to-seven-segment decoder?
 3.4 What is the way to obtain #6 (or 2, or3 and so on) on the display?
 3.5 Show the situation of segments from a to g on the display.
 3.6 If we apply +5V to segments b and c we can see #____ on the display.
 3.7 How many pins has the chip of seven-segment display got?
 3.8 What shall we do with pins #3, 5, 8?
 3.9 Show seven-segment display internal structure with LEDs.
 3.10 What is another name of a seven-segment display?
 3.11 What is the difference between conversion and coding of a decimal number?
 3.12 Show the differences between 1- and 2-digit seven-segment display.

LAB WORK PERFORMANCE.

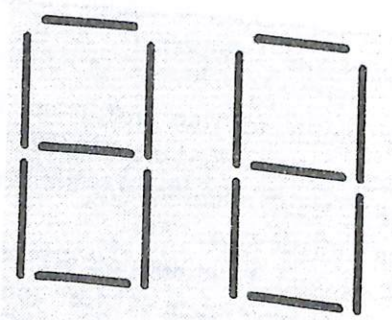
1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount the scheme of experiment 4A on the breadboard and perform it.
5. Make a conclusion about functionality of the scheme. Compare your results with theoretical ones.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Mount the scheme of experiment 4B on the bread board. Use 2-digit seven-segment display of common cathode type.
8. Find which pin corresponds to appropriate segment, and fill in the table.
9. Repeat steps 7 and 8 for experiment 4C. Use another type of seven-segment display.
10. Be ready to answer your instructor's questions in process of work.
11. Complete your work, dismount your scheme, and clean your working place.
12. Answer your instructor's final questions, obtain your mark.
13. Ask your instructor's permission to leave.

Experiment 4A. Realize the following circuit on a breadboard. Connecting Va, Vb, Vc, Vd, Ve, Vf and Vg inputs to either GND or VCC based on the following table, fill in the blanks.



	Va	Vb	Vc	Vd	Ve	Vf	Vg	Display
1	5V	5V	5V	5V	5V	5V	0V	0
2	0V	5V	5V	0V	0V	0V	0V	1
3	5V	5V	0V	5V	5V	0V	5V	2
4	5V	5V	5V	5V	0V	0V	5V	3
5	0V	5V	5V	0V	0V	5V	5V	4
6	5V	0V	5V	5V	0V	5V	5V	5
7	0V	0V	5V	5V	5V	5V	5V	6
8	5V	5V	5V	0V	0V	0V	0V	7
9	5V	5V	5V	5V	5V	5V	5V	8
10	5V	5V	5V	0V	0V	5V	5V	9
11	5V	0V	5V	5V	0V	5V	5V	5
12	0V	5V	5V	5V	5V	0V	5V	d
13	0V	5V	5V	5V	5V	0V	5V	0

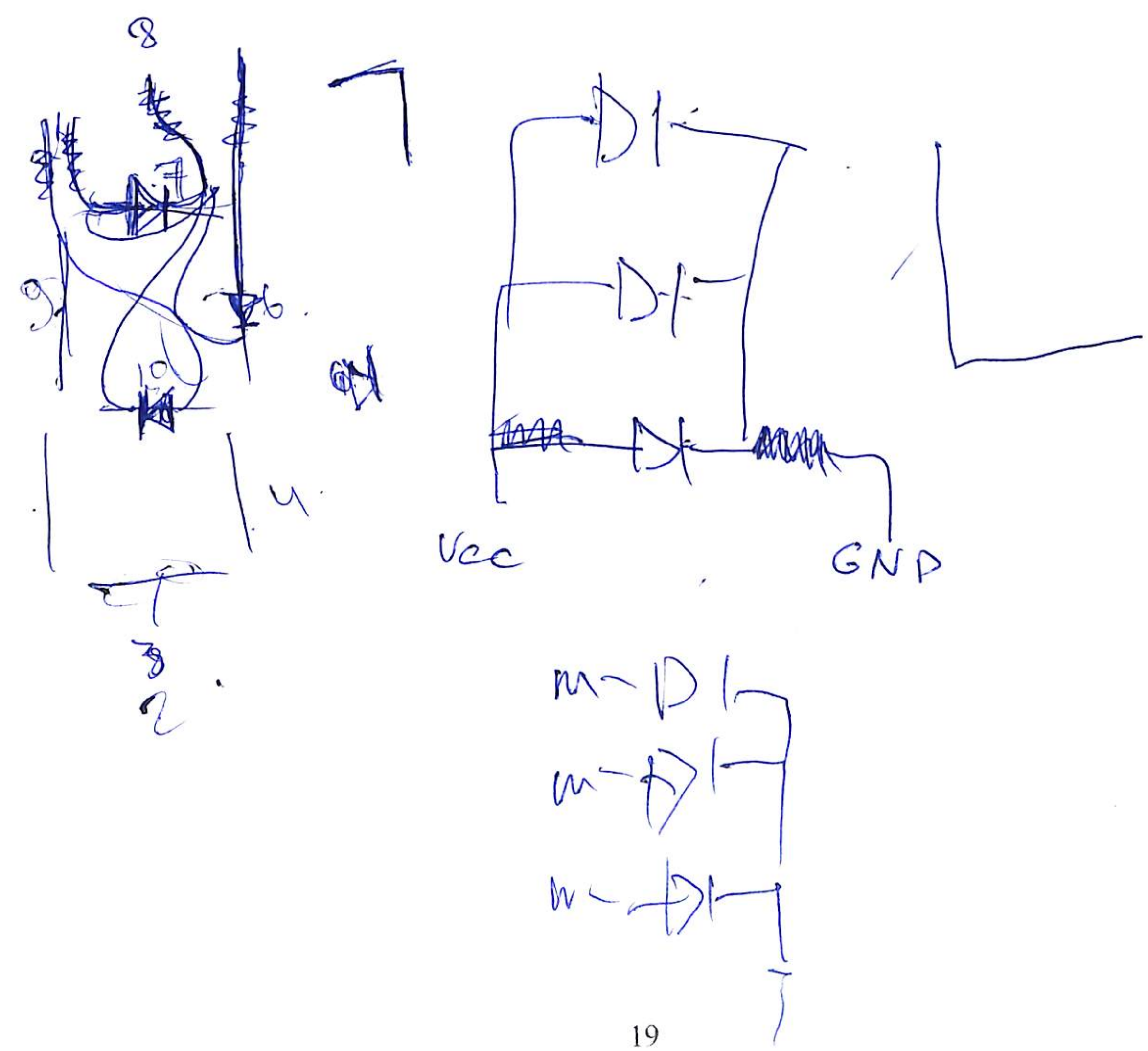
Experiment 4B. Use 2-digit seven- segment display. Situate it on the breadboard. Pins 13 and 14 are connected to GND. Define which pin corresponds to which segment, show them in the picture. Fill in the table, showing the voltage for the numbers obtained. For example, V_1 is voltage, applied to pin 1 and so on. Use resistors of 330(220)Ω to avoid the LED's burning.



#	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_{10}	V_{11}	V_{12}	V_{15}	V_{16}	V_{17}	V_{18}	[illegible]
1																	[illegible]
2																	[illegible]
3																	[illegible]
4																	[illegible]
5																	[illegible]
6																	[illegible]
7																	[illegible]
8																	[illegible]
9																	[illegible]
10																	[illegible]

Experiment 4C. Use another type of 2-digit seven segment display (common anode). Make appropriate connections and fill in the table.

#	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_{10}	V_{11}	V_{12}	V_{15}	V_{16}	V_{17}	V_{18}	#
1																	15
2																	24
3																	37
4																	60
5																	89
6																	41
7																	52
8																	73
9																	96
10																	08



TEST QUESTIONS

1. What fragment corresponds to definition of the Gray code?

A

x	y	F
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

B

x	y	F
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1

C

x	Y	F
0	0	0
0	0	1
0	1	1
0	1	0
1	0	0

D

x	y	F
0	0	0
1	0	0
1	0	1
1	1	0
1	1	1

E

x	y	F
0	0	0
1	0	0
1	1	1
1	1	0
1	0	1

2. A code converter is a circuit that
   A. makes the several systems compatible
   B. makes the two systems compatible
   C. makes the two systems compatible even though each uses a different binary code
   D. makes the two systems compatible even though each uses a different codes
   E. makes the several systems compatible even though each uses a different binary code

3. Decimal 3 will be represented in 8,4,-2,-1 code as
   A. 0111 B. 0101 C. 0110 D. 0100 E. 1000

4. What factor is, as a rule, more important for the circuit?
   A. number of gates B. Types of gates C. Propagation delay
   D. number of levels of implementation D. None of above mentioned

5. In biquinary code decimal 2 is
   A. 0100100 B. 0010010 C. 0100101 D. 1000010 E. 1000001

6. Binary conversion of decimal 12 is ________, the coding it in BCD is ______.
   A. 1101, 00010011 B. 1101, 1100 C. 1101, 1111 D. 1100, 01101100
   E. 1100, 00010010

7. In the table below you can see a message. Show the parity bit for rows 1 to 3 if odd parity system is adopted.
   A. 0,0,1 B. 1,0,1 C. 1,1,0 D. 0,1,0 E. 0,1,1

Message	Parity bit
0001	
1110	
0110	

8. Decimal 1 will be represented in Excess-3 code as
   A. 0111 B. 0101 C. 0110 D. 0100 E. 1110

9. Binary combination of decimal 5 in Excess -3 code means decimal ______ for 8,4,-2,-
   code.
   A. 2 B. 3 C. 4 D. 6 E. 8

10. Decimal 9 will be represented in 2,4,2,1 code as
   A. 0111 B. 0101 C. 0110 D. 1100 E. 1111

LABORATORY WORK # 5.

FOUR-BIT BINARY PARALLEL ADDER.

Aims: investigate 4-bit binary parallel adder operation; make an addition according to the task. Compare the results of the addition with ones, made by theoretical way.

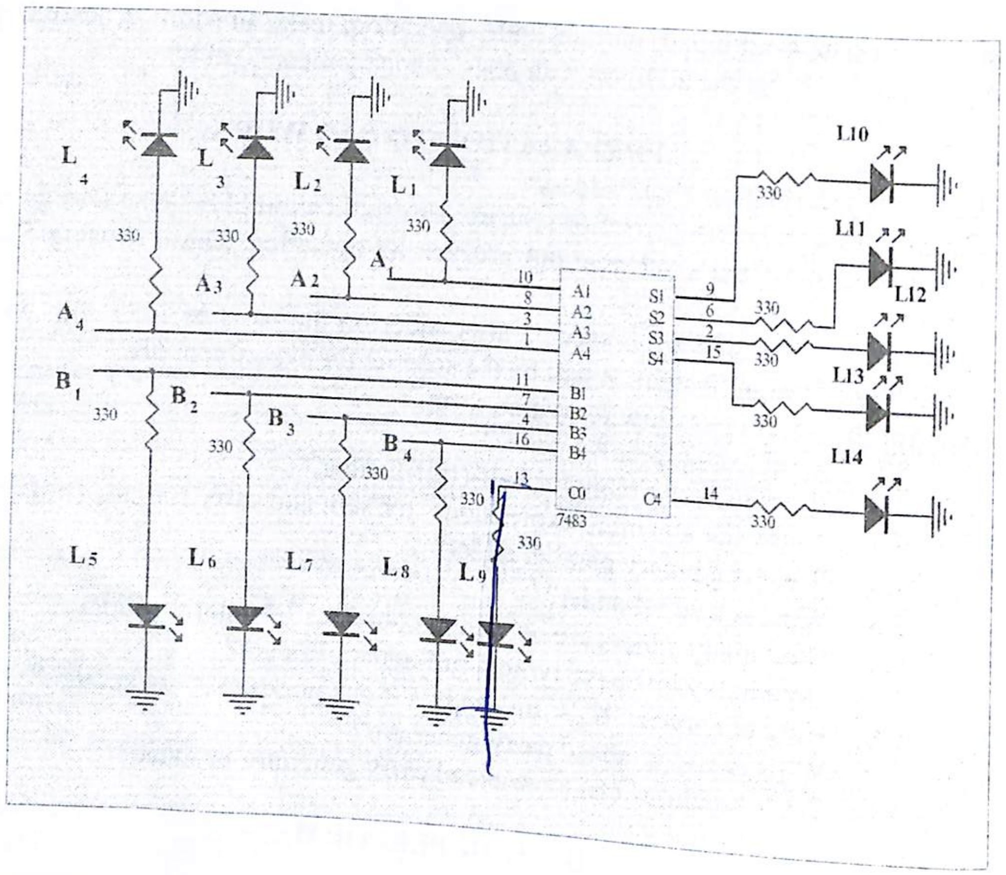
PREPARATION TO LAB WORK.

1 Learn the information about adders.
2 Draw look-ahead carry generator scheme with application of Scheme Design System.
3 Consider experiment's scheme and analyze its operation. Draw it using Scheme Design System.
4 Draw the scheme of 8-bit binary parallel adder on the basis of 7483 chip with application of Scheme Design System. It will be the scheme for experiment 5B.
5 Answer the questions below in written form.
   5.1 What is a half-(full-) adder?
   5.2 Show the truth table for half-(full-) adder.
   5.3 Show the algebraic expressions for sum and carry for half-(full-) adder.
   5.4 What is a binary parallel adder?
   5.5 What is a serial adder?
   5.6 How many adders are needed to construct 7-bit parallel adder?
   5.7 How many bits have typical full-adders ICs got?
   5.8 How to connect IC's full-adders if one package is not enough?
   5.9 What is a look-ahead carry generator?
   5.10 What functions can look-ahead carry generator produce?

LAB WORK PERFORMANCE.

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount the scheme of experiment 5A on the breadboard and perform it.
5. Make a conclusion about functionality of the scheme. Compare your results with theoretical ones.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Repeat steps 4 to 6 for experiment 5B.
8. Be ready to answer your instructor's questions in process of work.
9. Complete your work, dismount your schemes, clean your working place.
10. Answer your instructor's final questions, obtain your mark.
11. Ask your instructor's permission to leave.

Experiment 5A. Realize the following circuit on a breadboard. Connecting A and B inputs t either GND (for 0) or VCC (for 1) based on the following table, fill in the blanks. Connect p 5 of 7483 to VCC and pin 12 to GND. Write ON or OFF for LEDs.



Numbers for addition								inputs									outputs				
A1	A2	A3	A4	B1	B2	B3	B4	L1	L2	L3	L4	L5	L6	L7	L8	L9	L 10	L 11	L 12	L 13	L 14
1	1	0	0	1	1	0	1	1	1			1			1		1		1	1	
0	0	0	1	1	1	1	1				1	1	1	1	1					1	1
1	0	0	1	0	1	1	0	1					1	1							1

Experiment 5B. Do the same things for your own circuit for 8-bit addition. Add numbers 00101100 and 11000100, 11101100 and 11001100.

TEST QUESTIONS

1. Name the inputs______ and outputs_________ of a half-adder.
   A. A_0, B_0, C_{in}, Σ_0 B. A_0, B_0, C_{out}, Σ_0 C. C_{in}, Σ_0 A_0, B_0 D. C_{out}, Σ_0 A_0, B_0,
   E. Σ_0 A_0, B_0

2. The first strip to obtain resistance 220 Ω must be
   A. white B. Green C. Brown D. Yellow E. red

3. What statement is wrong?
   A. (X+Y)(X+Z)=X+YZ B. X(Y+Z)=XY+XZ C. X+XY=X
   D. (X+Y)′=X′Y′ E. X(X+Y)=X+Y

4. A Boolean function is an expression, formed with
   A. binary numbers
   B. binary variables
   C. binary variables and operators
   D. binary variables, the two binary operators OR and AND, the unary operator NOT, parentheses, and equal sign.
   E. binary variables, the binary operators OR, AND, and NOT, parentheses, and equal sign.

5. 7483 is
   A. 3*8 decoder B. 4-bit magnitude comparator C. Code converter
   D. 4-bit full adder E. priority encoder

6. What factor is, as a rule, more important for the circuit?
   A. number of gates B. Types of gates C. Propagation delay
   D. number of levels of implementation D. None of above mentioned

7. Serial binary adder consists of
   A. n full adders, connected in cascade, where n-number of digits for addition
   B. n half adders, connected in cascade, where n-number of digits for addition
   C. n full adders and a storage device, where n-number of digits for addition
   D. n half adders and a storage device, where n-number of digits for addition
   E. one full adder and a storage device

8. A half-subtractor is a ________ circuit, that subtracts ________ bits and produces their difference.
   A. sequential; three
   B. sequential; two
   C. combinational; two
   D. combinational; three
   E. sequential or combinational; three

9. Make addition of binary numbers: 1001 and 1010. Result is
   A. 10011 B. 1001 C. 1100 D. 11001 E. 10101

10. To construct 6-bit parallel adder we must use cascade of such full-adders IC s as
    A. two 2-bit and one 1-bit B. one 2-bit and one 3-bit C. one 4-bit and one 1-bit
    D. five 1-bit E. none of above mentioned, because 5-bit parallel adder IC exists itself

LABORATORY WORK # 6.

BCD ADDER.

Aims: investigate BCD adder operation, make an addition according to the task. Compare results of the addition with ones, made by theoretical way.

PREPARATION TO LAB WORK.

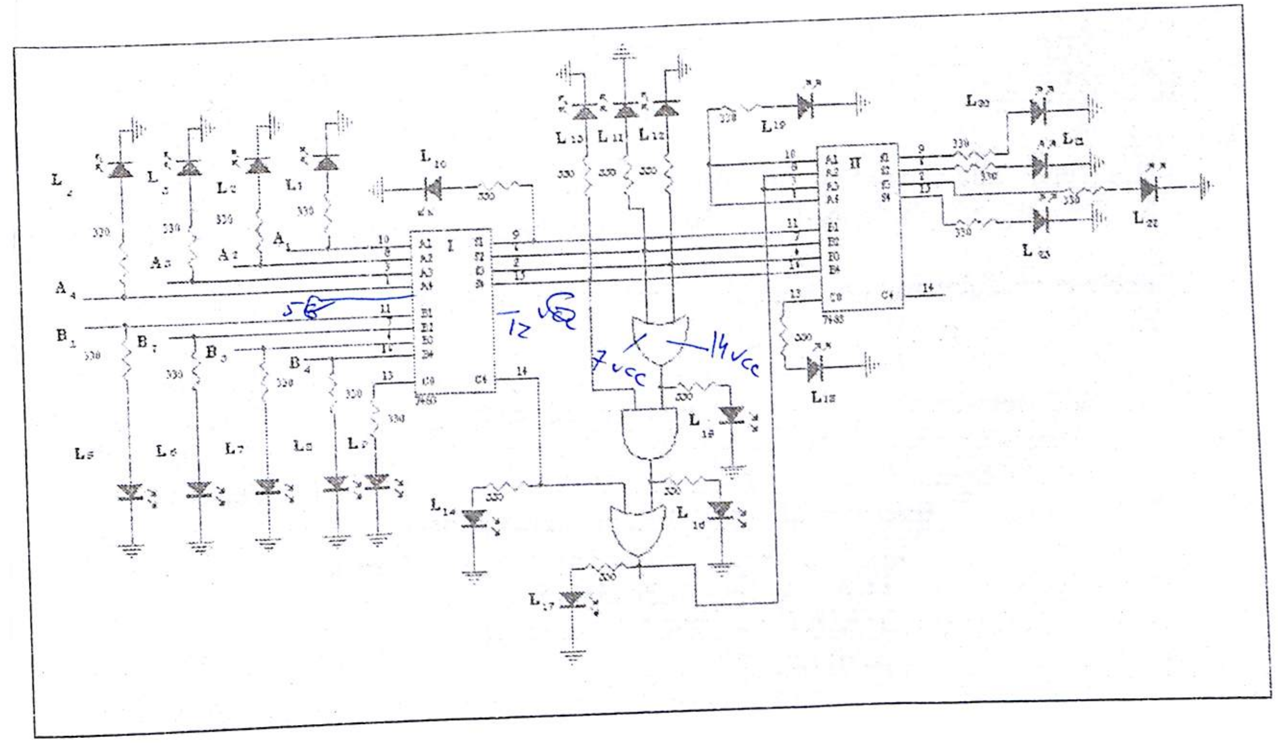
1. Learn the information about BCD adder and combinational logic.
2. Draw block diagram of a BCD adder with application of Scheme Design System compare this scheme with a scheme of experiment #6.
3. Answer the questions below in written form.
   3.1. What is a decimal adder?
   3.2. What is a BCD adder?
   3.3. For what purpose do 3 external gates exist in the scheme of BCD adder?

LAB WORK PERFORMANCE.

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount the scheme of experiment 6 on the breadboard and perform it.
5. Make a conclusion about functionality of the scheme. Compare your results w theoretical ones.
6. Demonstrate your results to your instructor. If your results are correct you m dismount your scheme, if no – find the mistake.
7. Be ready to answer your instructor's questions in process of work.
8. Complete your work, dismount your schemes, clean your working place.
9. Answer your instructor's final questions, obtain your mark.
10. Ask your instructor's permission to leave.

Experiment 6. Realize the circuit on a breadboard. For 2-input AND take 7408, pins 1,2-inputs, pin 3 output. For 2-input OR take 7432, pins 1,2,4,5-inputs, pins 3,6-outputs. Fill in the tables. Connect pin 5 of 7483 to VCC and pin 12 – to GND. Show ONs or OFFs for LEDs.

Tasks for addition:



options	Inputs of basic adder									Outputs of basic adder				
	L_1	L_2	L_3	L_4	L_5	L_6	L_7	L_8	L_9	L_{10}	L_{11}	L_{12}	L_{13}	L_{14}
5+9	on	off	on	off	on	off	on	off	on	off	on	on	on	off
7+8	on	on	on	off	on	off	off	off		on	on	on	on	off
4+3	off	off	on	off	on	on	on	on		on	on	on	off	on

options	Inputs of correction adder					Outputs of the circuit			
	L_{15}	L_{16}	L_{17}	L_{18}	L_{19}	L_{20}	L_{21}	L_{22}	L_{23}
5+9	on	on	on		c	off	off	on	off
7+8	on	on	on			on	off	on	on
4+3	on	off	off			on	on	on	off

Conclusion:

TEST QUESTIONS

1. The content of register when we enter 249 in BCD is:

	0	0	1	0	0	1	0	0	1	0	0	1
B	0	0	1	0	0	1	0	0	1	0	0	1
C	0	1	0	0	0	0	1	0	1	0	0	0
D	0	0	1	1	0	1	0	0	1	0	0	1
E	0	0	1	0	0	0	1	1	1	0	0	1

2. A small-scale integration (SSI) device contains __________ gates in a single chip.
A. thousands of B. From10 to 1000 C. More than 100 D. From 10 to 100 E. less than

3. Number of functions of n variables can be determined according to the formula
A. 2^{2^n} B. 2^{2n} C. 2^n D. 2^{3^n} E. 2^{3n}

4. A half-subtractor is a ________ circuit, that subtracts ________ bits and produces their difference.
A. sequential; three B. sequential; two C. combinational; two
D. combinational; three E. sequential or combinational; three

5. What is the result of the following BCD addition?

```
  0011 0010 1001 0101
+      0111 0000 0110
```

A. 0011 1001 1001 1011 B. 0100 0000 0000 0001 C. 0011 1001 1001 0001
D. 0100 0000 0000 1011 E. 0011 0000 0000 1011

6. Add in octal: 541+326
A. 967 B. 867 C. 1067 D. 947 E. 948

7. Full adder forms __________, but half-adder forms __________.
A. the sum of two bits, …. the sum of two bits and a previous carry.
B. the sum of two bits, …. the sum of two bits and a carry
C. the sum of two bits, …. the sum of two bits and a present carry
D. the sum of two bits and a carry,… the sum of two bits
E. the sum of two bits and a previous carry, … the sum of two bits

8. Add in hex: A8D5+3CA9
A. D56D B. D56E C. D46D D. E56E E. E57E

9. A Boolean function is an expression, formed with
A. binary numbers
B. binary variables
C. binary variables and operators
D. binary variables, the two binary operators OR and AND, the unary operator NOT, parentheses, and equal sign.
E. binary variables, the binary operators OR, AND, and NOT, parentheses, and equal sign

10. Equation for carry output of the second stage of look-ahead carry generator is
A. $C_2=G_1+P_1C_1$ B. $C_2=G_1+P_1$ C. $C_2=G_1+C_1$ D. $C_2=G_1+P_2C_1$ E. $C_2=G_1+P_1C_2$

LABORATORY WORK # 7.

MAGNITUDE COMPARATOR.

Aims: investigate operation of the magnitude comparator as a MSI circuit.

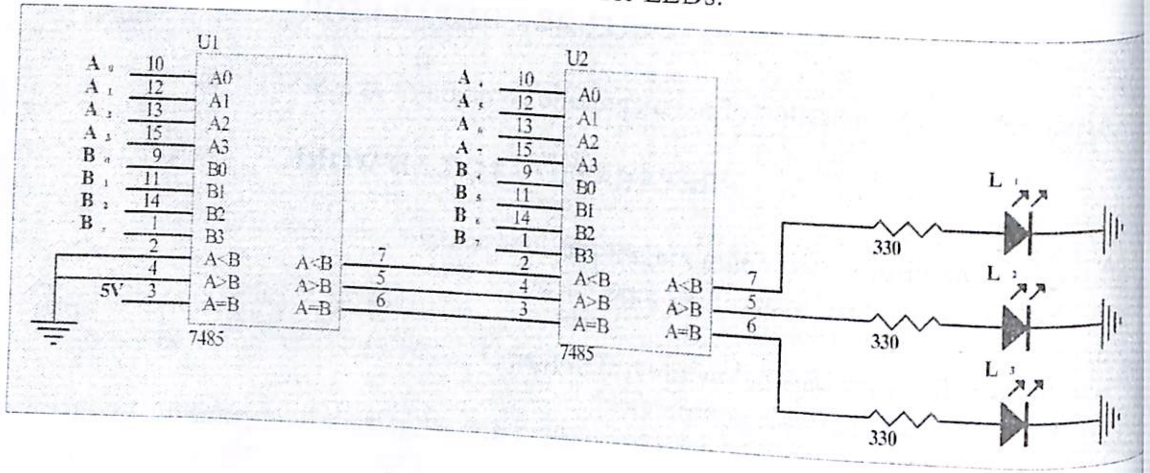
PREPARATION TO LAB WORK.

1. Learn the information about magnitude comparator.
2. Fill in the table for experiment theoretically.
3.
4. Answer the questions below in written form.
   4.1. What is magnitude comparator?
   4.2. How many output signals may exist for magnitude comparator simultaneously and why?
   4.3. Why A<B, A>B inputs of the first 7485 must be grounded?
   4.4. Why A=B input of the first 7485 must be HIGH?
   4.5. What are outputs of the first 7485 if numbers for comparison are 00110111 and 00100101?
   4.6. Show the scheme which is suitable to define if 4-bit binary number A is equal to the 4-bit binary number B (use Scheme Design System).

LAB WORK PERFORMANCE.

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount the scheme of experiment 7 on the breadboard and perform it.
5. Make a conclusion about functionality of the scheme. Compare your results with theoretical ones.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Be ready to answer your instructor's questions in process of work.
8. Complete your work, dismount your schemes, clean your working place.
9. Answer your instructor's final questions, obtain your mark.
10. Ask your instructor's permission to leave.

Experiment 7. Prepare the circuit on the breadboard. Apply the signals according to the t[able] below. Fill in the gaps. Write down ON or OFF for LEDs.



#	Inputs																outputs		
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	L_1	L_2	L_3
1	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	0V	off	off	on
2	0V	0V	0V	0V	0V	0V	0V	5V	0V	0V	0V	0V	0V	0V	0V	0V	O	on	O
3	0V	0V	0V	0V	0V	0V	0V	5V	0V	0V	0V	0V	0V	0V	0V	5V	O	O	on
4	0V	5V	5V	0V	5V	5V	0V	0V	0V	5V	5V	0V	0V	2V	0V	0V	O	on	O
5	0V	5V	5V	0V	5V	5V	0V	0V	5V	5V	5V	0V	0V	2V	0V	0V	on	O	O
6	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	5V	O	O	on
7	5V	5V	5V	5V	5V	5V	5V	0V	5V	5V	5V	5V	5V	5V	5V	5V	on	O	O

7485 is a u bit magnitude comparator

Conclusion.

TEST QUESTIONS

1. The truth table for AND gate is:

A ✓

X	y	F
0	0	0
0	1	0
1	0	0
1	1	1

B

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

C

x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

D

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

E

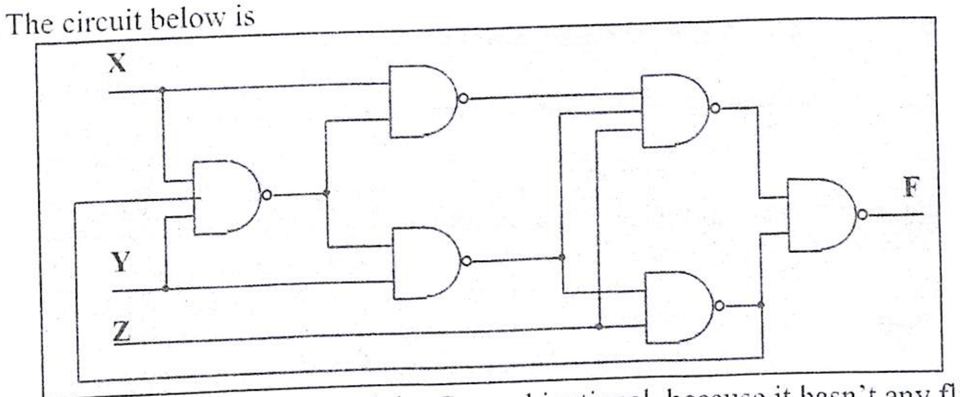
x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

2. Typical voltage for IC TTL logic family for negative logic is for HIGH - 5 V, for LOW- 0 V.
A. 0.2, 3.5 B. 3.5, 0.2 (C.) 5, 0 D. 0, 5 ✓E. 0, 3.5

3. Power dissipation is
A. the power consumed by the gate
(B.) the power consumed by the gate, which must be available from the power supply
C. the power consumed by the gate, which may be available from the power supply
D. the power emitted by the gate
E. the power emitted by the gate, which may be available for the gates of the next level

4. 7485 is
A. 3*8 decoder (B.) 4-bit magnitude comparator C. Code converter
D. D flip-flop E. priority encoder

5. The circuit below is



A. combinational B. sequential C. combinational, because it hasn`t any flip-flops
(D.) sequential, because it has a feedback path
✓E. sequential, because it has a feedback path between output and input

6. Function # ____ corresponds to function NOR of 3 variables.

X	Y	Z	F_1	F_2	F_3	F_4	F_5
0	0	0	0	0	0	0	1
0	0	1	0	0	1	1	0
0	1	0	0	0	1	1	0
0	1	1	1	1	1	1	0
1	0	0	0	1	1	1	0
1	0	1	1	1	1	0	0
1	1	0	1	1	1	0	0
1	1	1	1	1	1	1	0

A. 1 B. 2 ✓C. 3 D. 4 (E.) 5

7. $XY'+X'Y$ is algebraic expression of ________ function.
A. XOR B. XNOR C. NOR D. NAND E. AND

8. For 4-bit magnitude comparator if A>B function ________ must be realized ($x_i=A_iB_i+A`_iB`_i$).
A. $A_2B`_2+ x_2A_1B`_1+ x_2x_1A_0B`_0$
B. $A`_2B_2+ x_2A`_1B_1+ x_2x_1A`_0B_0$
C. $A_3B`_3+ x_3A_2B`_2+ x_3x_2A_1B`_1+ x_3x_2x_1A_0B`_0$
D. $A`_3B_3+ x_3A`_2B_2+ x_3x_2A`_1B_1+ x_3x_2x_1A`_0B_0$
E. all answers are wrong

9. What statement is correct?
A. Tabulation method is not applicable for functions of 4 variables
B. Number of different functions of two variables is equal to 8.
C. NOT is a binary operator
D. 4-bit magnitude comparator can be used for comparison of two BCD numbers.
E. Decoder with enable can be used as multiplexer

10. To answer the question if two 4-bit binary numbers are equal each other for the circuit enough to use ________
A. 4XOR gates
B. 4XNOR gates
C. 4XOR gates and one AND gate
D. 4XNOR gates and one 4-input AND gate
E. 4XNOR gates and one 4-input OR gate

LABORATORY WORK # 8.

DECODER AND DEMULTIPLEXER.

Aims: investigate operation of the 2*4 decoder with enable as a decoder and as a demultiplexer.

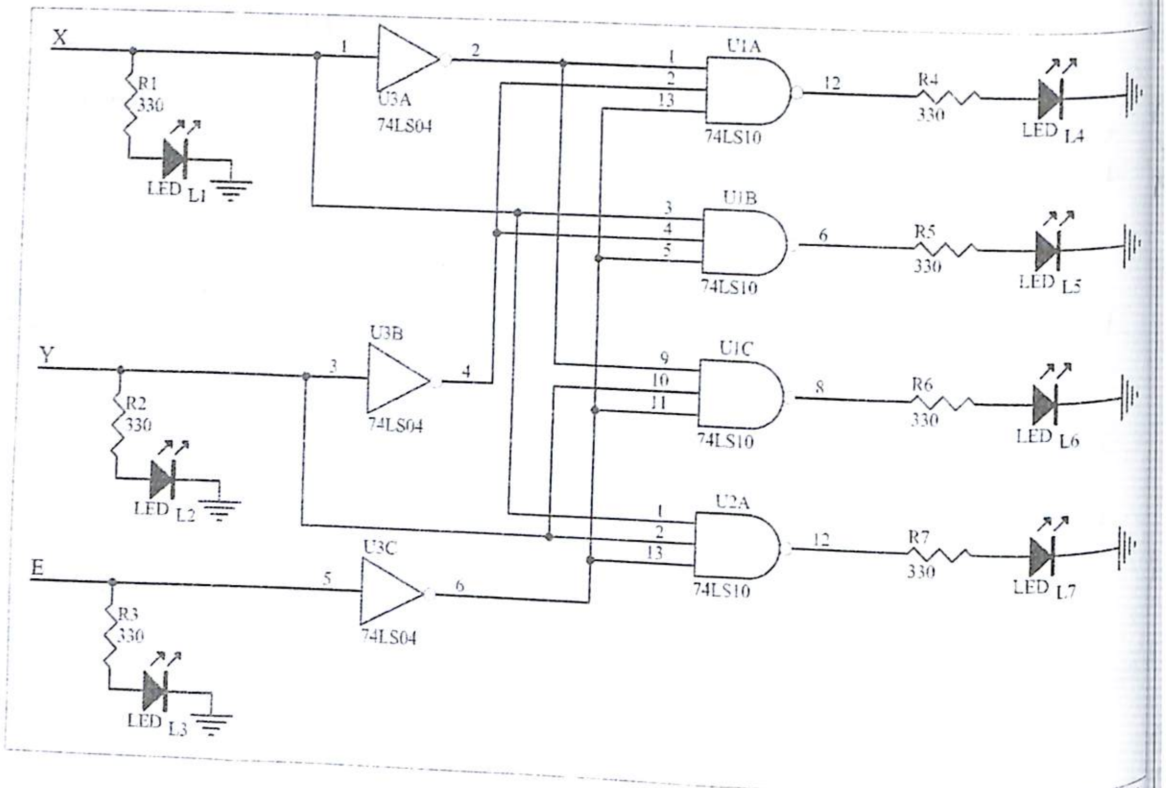
PREPARATION TO LAB WORK.

1. Learn the information about decoder and demultiplexer.
2. Consider the scheme of experiment 8A and define the results theoretically. Draw the scheme using Scheme Design System.
3. Construct 3*8 decoder using 2 decoder/demultiplexer ICs (74139) and an inverter for experiment 8B. Draw it using Scheme Design System.
4. Answer the question below in written form.
   4.1. What is a decoder?
   4.2. What is a DUX?
   4.3. Show the principal scheme of 2*4 decoder with application of Scheme Design System.
   4.4. What is enable input for a decoder?
   4.5. Decoder with an enable input can work as ________.
   4.6. Compare decoder and encoder.
   4.7. Compare DUX and MUX.
   4.8. Show the scheme of 2*4 decoder on the basis of NOR gates (use Scheme Design System).

LAB WORK PERFORMANCE.

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount the scheme of experiment 8A on the breadboard and perform it. Fill in table #1.
5. Make a conclusion about functionality of the scheme. Compare your results with theoretical ones.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Repeat steps 4-6 for the experiment 8B.
8. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
9. Be ready to answer your instructor's questions in process of work.
10. Complete your work, dismount your schemes, clean your working place.
11. Answer your instructor's final questions, obtain your mark.
12. Ask your instructor's permission to leave.

Experiment 8A. Realize the circuit below on the breadboard.



Table

	E	X	Y	LED1	LED2	LED3	LED4	LED5	LED6	LED7
				INPUTS			OUTPUTS			
1	0V	0V	0V				on			
2	0V	0V	5V		on			on		
3	0V	5V	0V	on						
4	0V	5V	5V	on	on				on	
5	5V	X	X			on				on

As a result, this truth table belongs to a ....

Experiment 8B. Construct 3*8 decoder using 2 decoder/demultiplexer ICs (74139) and an inverter. Mount the scheme on a breadboard and fill the table below.

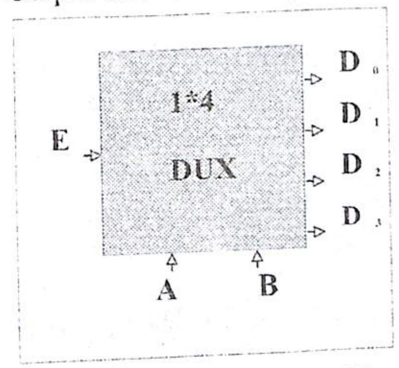
Table

	X	Y	Z	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11
				INPUTS			OUTPUTS							
1	0V	0V	0V											on
2	0V	0V	5V			on							on	
3	0V	5V	0V		on							on		
4	0V	5V	5V		on	on					on			
5	5V	0V	0V	on						on				
6	5V	0V	5V	on		on			on					
7	5V	5V	0V	on	on			on						
8	5V	5V	5V	on	on	on	on							

TEST QUESTIONS

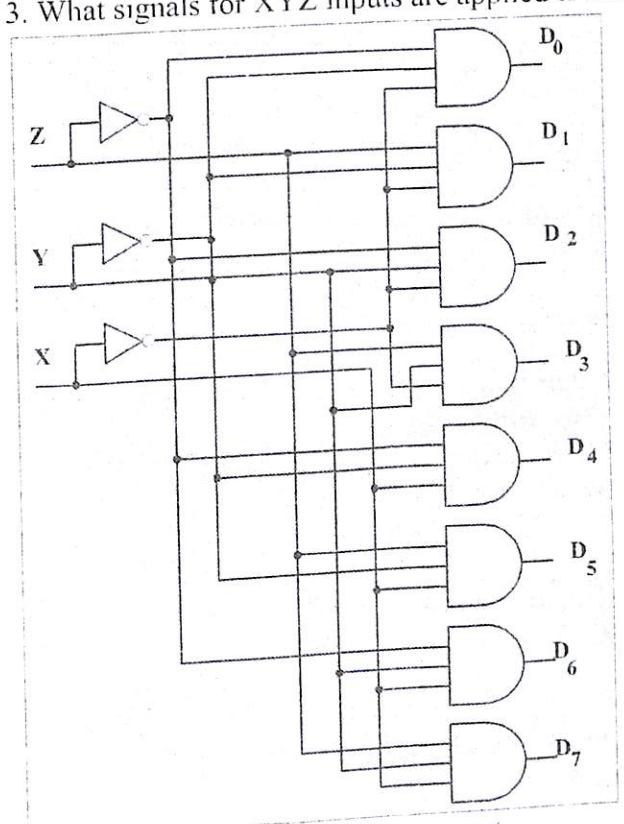
1. A decoder is a combinatioal circuit that
A. converts binary information from n input lines to a maximum of 2^n unique output lines
B. has 2^n (or less) unique input lines and n output lines
C. selects binary information from one of many input lines and direct it to a single output line
D. receives information on a single line and transmits this information on one of 2^n possible output lines
E. converts binary information from n input lines to m output lines

2. Output of 1*4 demultiplexer is D_1. What are selection lines?



A. 00 B. 01 C. 10 D. 11 E. any of them

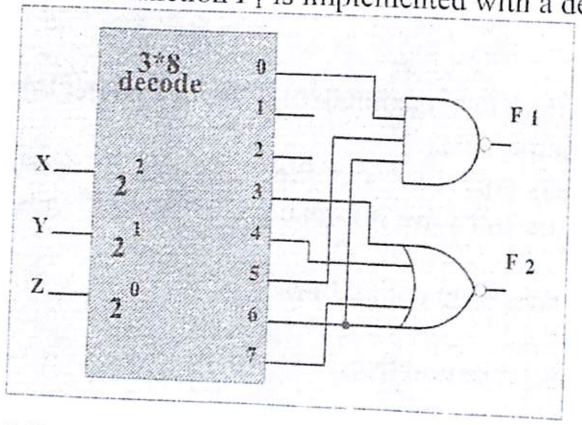
3. What signals for XYZ inputs are applied if active output is D_0?



A. 0, 0, 0
B. 0, 1, 1
C. 1, 0, 0
D. 0, 1, 0
E. 0, 0, 1

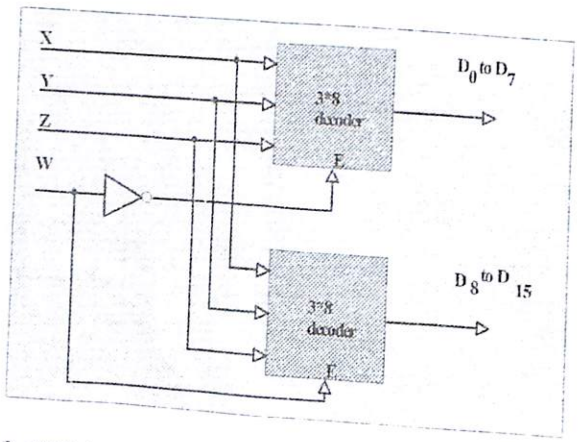
4. Decoder is ________ component.
A. SSI B. MSI C. LSI D. VLSI E. SSI or MSI

5. What function F_1 is implemented with a decoder and external gate?



6. What statement is correct?
A. A decoder can be realized on the basis of OR gates.
B. A decoder can be used as a MUX.
C. A decoder can be used as a data selector.
D. A 3-to-8 line decoder can be used for a binary-to-BCD conversion.
E. A 3-to-8 line decoder can be used for a binary-to-octal conversion.

7. What input signals must be applied to WXYZ for the circuit below if D_8 is generated as output?



8. Fill in the gaps.
If we use NAND gates for decoder the outputs will be active-_____. It means that only one output will be high at the moment, others will be Low.
A. HIGH, HIGH, LOW
B. HIGH, LOW, HIGH
C. LOW, HIGH, HIGH
D. LOW, LOW, HIGH
E. all answers are wrong

9. DUX sometimes is called
A. code converter
B. data selector
C. data distributor
D. decoder
E. all answers are correct

10. The scheme in question 3 is________.
A. 1-of-8 decoder
B. 3-to-8 line decoder
C. binary-to-octal decoder
D. A,B,C are correct
E. A,B,C are wrong

LABORATORY WORK # 9.

ENCODER.

Aims: investigate operation of the octal-to-binary encoder.

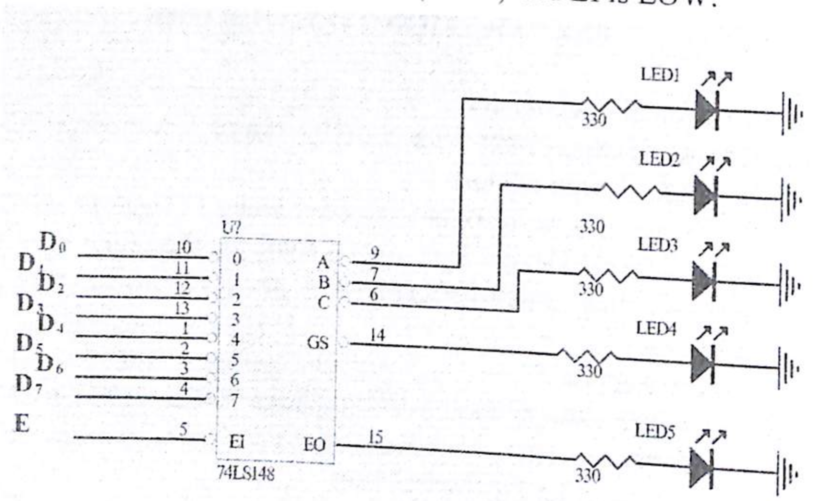
PREPARATION TO LAB WORK.

1. Learn the information about encoder
2. Consider the scheme of experiment 9A and define the results theoretically. Draw the scheme using Scheme Design System.
3. Implement the scheme of octal-to-binary encoder using OR gates and draw the scheme with application of Scheme Design System. This will be the scheme for the experiment 9B.
4. Answer the question below in written form.
   4.1. What is an encoder?
   4.2. What is a priority encoder?
   4.3. Show the principal scheme of octal-to-binary and explain why D_0 is not connected with any of OR gates.
   4.4. What discrepancy may be for this scheme?

LAB WORK PERFORMANCE.

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount the scheme of experiment 9A on the breadboard and perform it. Fill in the table.
5. Make a conclusion about functionality of the scheme. Compare your results with theoretical ones.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Repeat steps 4-6 for experiment 9B.
8. Be ready to answer your instructor's questions in process of work.
9. Complete your work, dismount your schemes, clean your working place.
10. Answer your instructor's final questions, obtain your mark.
11. Ask your instructor's permission to leave.

Experiment 9A. Realize the following circuit on a breadboard. Connecting D_0-D_7 to GND or VCC based on the following table, fill in the blanks. Write ON or OFF for LEDs. Remember that EI is active LOW enable input: a HIGH on this input forces all outputs to their inactive (HIGH) state; EO is active-LOW enable output: this output pin goes LOW when all inputs are inactive (HIGH) and EI is LOW; GS is active-LOW group signal output: this output pin goes LOW whenever any of the inputs are active (LOW) and EI is LOW.



		INPUTS									OUTPUTS				
		(EI)'	D0'	D1'	D2'	D3'	D4'	D5'	D6'	D7'	GS'	A	B	C	EO'
	1	5	X	X	X	X	X	X	X	X	+	+	+	+	+
	2	0	5	5	5	5	5	5	5	5		+	f	+	+
	3	0	X	X	X	X	X	X	X	0					+
	4	0	X	X	X	X	X	X	0	5				+	+
	5	0	X	X	X	X	X	0	5	5			+		f
	6	0	X	X	X	X	0	5	5	5			f	+	+
	7	0	X	X	X	0	5	5	5	5			+		+
	8	0	X	X	0	5	5	5	5	5		+		f	+
	9	0	X	0	5	5	5	5	5	5		f	+	+	f
	10	0	0	5	5	5	5	5	5	5		f	+	+	f

Experiment 9B. Implement the scheme of octal-to-binary encoder using OR gates and mount it on the breadboard. Fill in the table below. Compare your results with the table above.

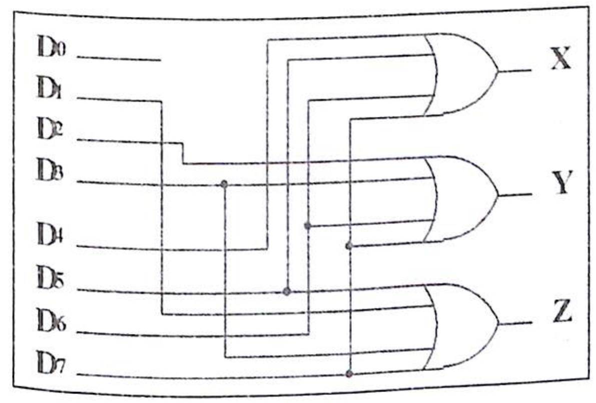
		INPUTS								OUTPUTS		
		D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	A	B	C
	1	5	0	0	0	0	0	0	0			
	2	0	5	0	0	0	0	0	0			
	3	5	5	0	0	0	0	0	0			
	4	0	0	5	0	0	0	0	0			
	5	0	5	5	0	0	0	0	0			
	6	0	0	5	0	0	5	0	0			
	7	0	0	0	5	0	0	0	0			
	8	0	0	0	0	5	0	0	0			
	9	0	0	5	5	5	5	5	5			
	10	0	5	5	5	5	5	5	5			

Conclusion.

TEST QUESTIONS

1. An encoder is a combinational circuit that
A. converts binary information from n input lines to a maximum of 2^n unique output lines
B. has 2^n (or less) unique input lines and n output lines
C. selects binary information from one of many input lines and direct it to a single output line
D. receives information on a single line and transmits this information on one of 2^n possible output lines
E. converts binary information from n input lines to m output lines

2. If D_1 is active input outputs XYZ will be ______

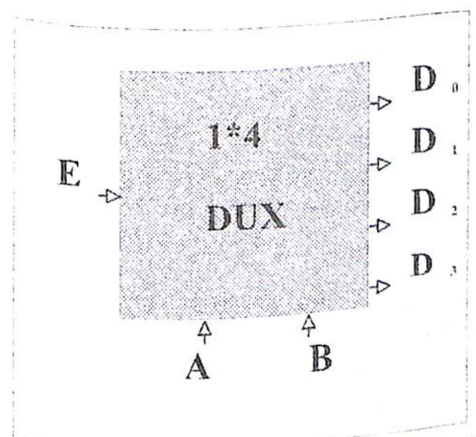


A. 111
B. 100
C. 101
D. 011
E. 001

3. 74139 is
A. decoder
B. DUX
C. MUX
D. dual 2-to-4 line decoder
E. triple 3-input NAND gate

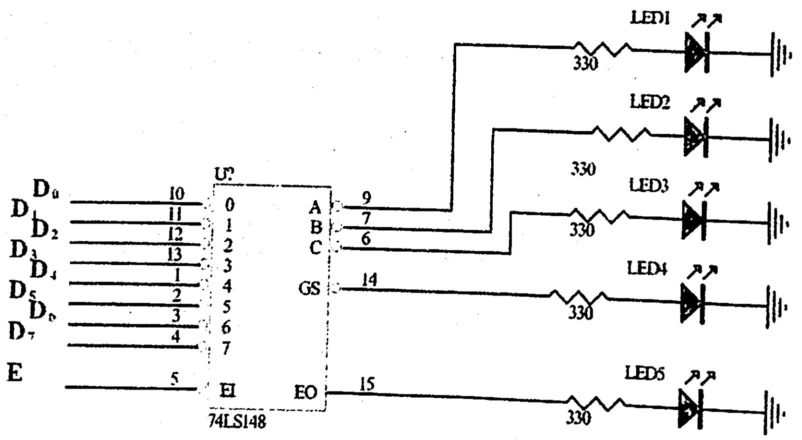
4. DUX sometimes is called
A. code converter
B. data selector
C. data distributor
D. decoder
E. all answers are correct

5. What output of 1*4 demultiplexer will be chosen if selection lines AB=00?



A. D_1 B. D_0 C. D_2 D. D_3 E. any of them

6. For the circuit below if EI=5V, D_1=0, D_5=0 the state of L_1 to L_5 will be:



A. ON,ON,ON,ON,ON B. OFF,OFF,OFF,ON,ON
C. ON,ON,ON,OFF,OFF D. OFF,OFF, ON,ON,ON,
E. OFF, ON,ON,ON, OFF

7. For the circuit in question 6 if EI=0, D_0 to D_7=5V the state of L_1 to L_5 will be:
A. ON,ON,ON,ON,OFF B. OFF,OFF,OFF,ON,ON
C. ON,ON,ON,OFF,OFF D. OFF,OFF, ON,ON,ON,
E. OFF, ON,ON,ON, OFF

8. For the circuit in question 6 enable input is active-______. A _____ on this input forces all outputs to their inactive _____ state.
A. LOW, HIGH, LOW B.LOW, LOW, HIGH,
C. HIGH, LOW, HIGH D. HIGH, HIGH, LOW E. LOW, HIGH, HIGH

9. For priority encoder we have got input lines D_1, D_3, and D_6 active simultaneously. In such case output signal will be corresponded to …
A. D_1 B. D_3 C. D_6 D. D_1or D_3 E. D_3 or D_6

10. For the circuit in question 6 output signals are: L_1 is ON, L_2 is ON, L_3 is ON, GS is OFF, EO is ON. It means that
A. the chip is disabled B. any input signal is absent
C. number 7 is encodered D. number 0 is encodered
E. all answers are wrong

LABORATORY WORK # 10.

MULTIPLEXER.

Aims: investigate operation of the 8*1 multiplexer.

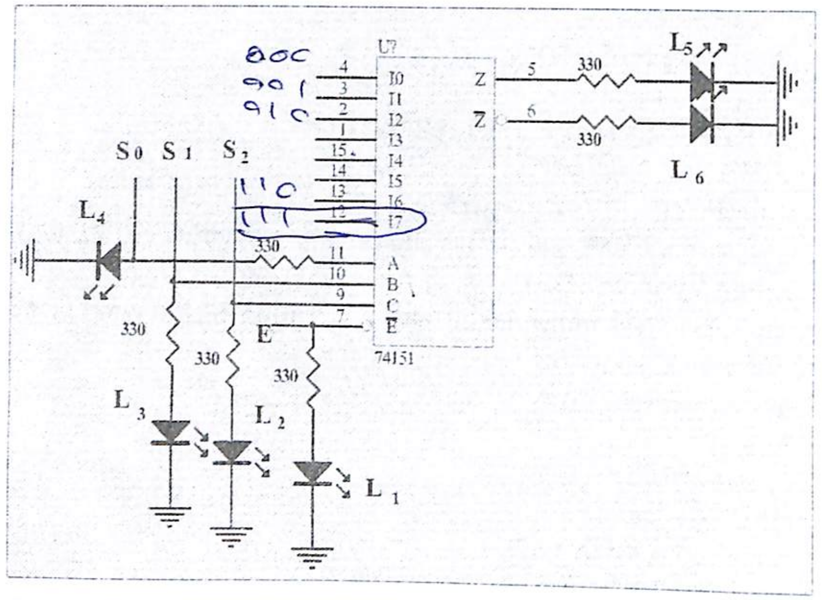
PREPARATION TO LAB WORK.

1. Learn the information multiplexer
2. Consider the scheme of experiment 10A and define the results theoretically. Draw the scheme using Scheme Design System (SDS).
3. Construct and draw (using SDS) 16*1 multiplexer with 2 8*1 multiplexers and an OR gate. This will be the scheme for experiment 10B
4. Answer the question below in written form.
   - 4.1. What is a MUX?
   - 4.2. A MUX's another name is _________
   - 4.3. Enable input of a MUX is called________.
   - 4.4. How many functions can a MUX realize?
   - 4.5. A MUX can be used as a DUX. True or false? Why?
   - 4.6. What is a role of a MUX's selection lines?

LAB WORK PERFORMANCE.

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount the scheme of experiment 10A on the breadboard and perform it. Fill in the table.
5. Make a conclusion about functionality of the scheme. Compare your results with theoretical ones.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Repeat steps 4-6 for experiment 10B.
8. Be ready to answer your instructor's questions in process of work.
9. Complete your work, dismount your schemes, clean your working place.
10. Answer your instructor's final questions, obtain your mark.
11. Ask your instructor's permission to leave.

Experiment 10A. Realize the following circuit on a breadboard. Connecting I_0-I_7 to GND or VCC based on the following table, fill in the blanks (X-don't –care conditions). Write ON or OFF for LEDs.



N	Inputs												outputs	
	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	E	S_2	S_1	S_0	Z	Z'
									L_1	L_2	L_3	L_4	L_5	L_6
1	0	5V	5V	0	5V	5V	0	5V	0	0	0	0		
2	0	5V	5V	0	5V	5V	0	5V	0	0	0	5V		+
3	0	5V	5V	0	5V	5V	0	5V	0	0	5V	0	+	+
4	0	5V	5V	0	5V	5V	0	5V	0	0	5V	5V	+	
5	0	5V	5V	0	5V	5V	0	5V	0	5V	0	0		+
6	0	5V	5V	0	5V	5V	0	5V	0	5V	0	5V	+	+
7	0	5V	5V	0	5V	5V	0	5V	0	5V	5V	0	+	+
8	0	5V	5V	0	5V	5V	0	5V	0	5V	5V	5V		+
9	5V	0	0	0	0	0	5V	5V	0	0	0	0	+	+
10	5V	0	0	0	0	0	5V	5V	0	0	0	5V	+	+
11	5V	0	0	0	0	0	5V	5V	0	0	5V	0		+
12	5V	0	0	0	0	0	5V	5V	0	0	5V	5V	+	+
13	5V	0	0	0	0	0	5V	5V	0	5V	0	0		+
14	5V	0	0	0	0	0	5V	5V	0	5V	0	5V		+
15	5V	0	0	0	0	0	5V	5V	0	5V	5V	0		+
16	5V	0	0	0	0	0	5V	5V	0	5V	5V	5V	+	+
17	5V	0	0	0	0	0	5V	5V	5V	X	X	X	+	+
18	5V	0	0	0	0	0	5V	5V	5V	X	X	X		+
19	5V	0	0	0	0	0	5V	5V	5V	X	X	X		+

Experiment 10B. Construct and mount 16*1 multiplexer with 2 8*1 multiplexers and an OR gate. Define how should inputs I_0-I_{15} be connected so that the output of the circuit (Z) would match the table below, which shows the relation between configuration of selection lines (S) and output of the circuit (Z).

S	5	1	12	7	6	8	15	9	0	3	11	2	4	10	13	14
Z	1	1	0	0	0	1	0	1	1	1	0	1	1	1	0	1

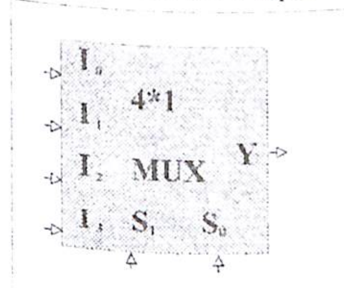
Conclusion.

TEST QUESTIONS

1. A multiplexer is a combinational circuit that
A. converts binary information from n input lines to a maximum of 2^n unique output lines
B. has 2^n (or less) unique input lines and n output lines
C. selects binary information from one of many input lines and direct it to a single output line
D. receives information on a single line and transmits this information on one of 2^n possible output lines
E. converts binary information from n input lines to m output lines

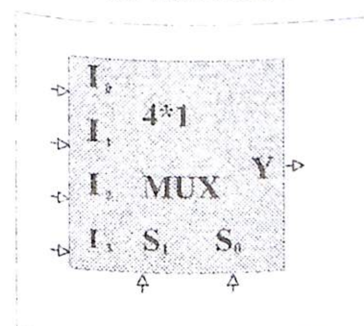
2. Strobe is
A. enable input of decoder
B. disable input of decoder
C. enable input of multiplexer
D. disable input of demultiplexer
E. disable input of multiplexer

3. What will the output signal of 4*1 multiplexer be if selection lines S_1S_0=11?



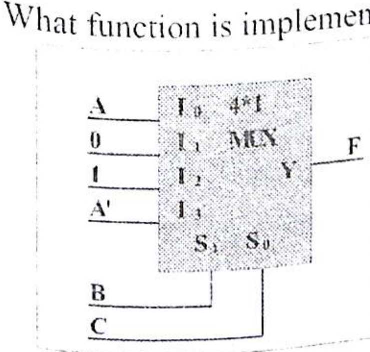
A. I_0
B. I_1
C. I_2
D. I_3
E. any of them

4. What are selection lines of 4*1 multiplexer if output signal $Y=I_1$?



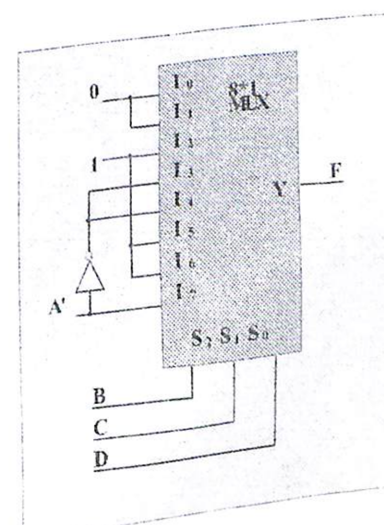
A. 00
B. 01
C. 10
D. 11
E. any of them

5. What function is implemented with multiplexer?



A. F(A,B,C)=Σ(2,3,5,6)
B. F(A,B,C)=Σ(1,3,5,6)
C. F(A,B,C)=Σ(2,3,5,7)
D. F(A,B,C)=Σ(2,3,4,6)
E. F(A,B,C)=Σ(1,3,5,7)

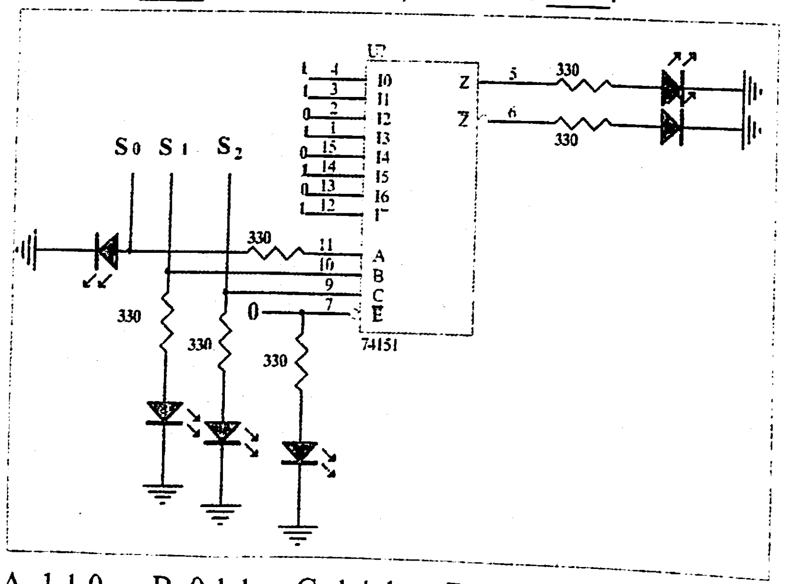
6. What function is implemented with multiplexer?



A. F(A,B,C,D)= Σ(2,5,6,7,10,11,12,13,14)
B. F(A,B,C,D)= Σ(0,1,3,4,7,14)
C. F(A,B,C,D)= Σ(0,1,3,4,8,15)
D. F(A,B,C,D)= Σ(0,1,3,4,8,9,15)
E. F(A,B,C,D)= Σ(0,1,3,5,7,14,15)

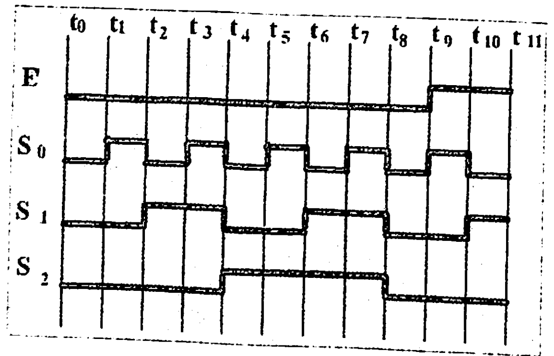
7. Decoder is __________ component.
A. SSI   B. MSI   C. LSI   D. VLSI   E. SSI or MSI

8. For the circuit below if selection lines $S_2S_1S_0$=011 the output Z will be ____, if $S_2S_1S_0$=100, Z will be ____, if $S_2S_1S_0$=001, Z will be ____.



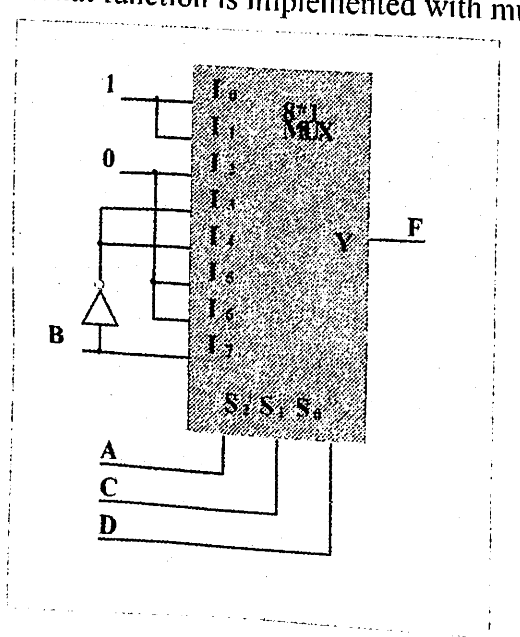
A. 1,1,0   B. 0,1,1   C. 1,1,1   D. 0,1,0   E. 1,0,1

9. For the circuit in question 8 the output Z is equal to _____ for periods of time between t_3 and t_4, t_4 and t_5, t_5 and t_6.



A. 0,1,1   B. 0,1,0   C. 1,1,1   D. 0,0,1   E. 1,0,1

10. What function is implemented with multiplexer?



A. F(A,B,C,D)= Σ(0,1,3,4,5,8,15)

B. F(A,B,C,D)= Σ(0,1,3,4,7,14)

C. F(A,B,C,D)= Σ(0,1,3,4,8,15)

D. F(A,B,C,D)= Σ(0,1,3,4,8,9,15)

E. F(A,B,C,D)= Σ(0,1,3,5,7,14,15)

LABORATORY WORK # 11.

D- FLIP-FLOP.

Aims: investigate operation of the D-flip-flop.

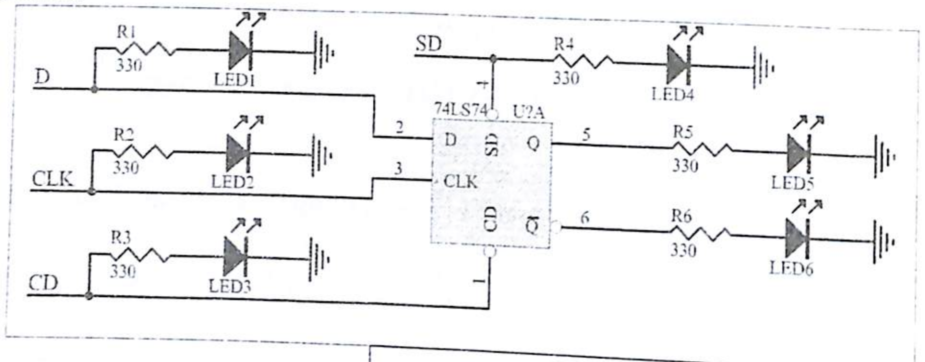
PREPARATION TO LAB WORK.

1. Learn the information about flip-flops.
2. Consider the scheme of experiment 11A and define the results theoretically. Draw the circuit with application of Scheme Design System.
3. Draw the D-flip-flop implemented with NAND gates (using Scheme Design System) for the experiment 11B.
4. Answer the question below in written form.
   - 4.1. What circuit is called sequential?
   - 4.2. What sequential circuit is called synchronous?
   - 4.3. What sequential circuit is called asynchronous?
   - 4.4. What is a master-clock generator?
   - 4.5. What circuits are called clocked sequential circuits?
   - 4.6. What is a flip-flop?
   - 4.7. What types of flip-flops do you know?
   - 4.8. Show truth tables for all types of flip-flops.
   - 4.9. Show the typical schemes of RS, D, T, JK-flip-flops and describe their operation. (Use Scheme Design System).
   - 4.10. What is a master-slave flip-flop?
   - 4.11. What is setup time and hold time for flip-flop?
   - 4.12. Show excitation tables for all types of flip-flops.
   - 4.13. What types of flip-flops' triggering do you know?

LAB WORK PERFORMANCE.

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount the scheme of experiment 11A on the breadboard and perform it. Fill in the table.
5. Make a conclusion about functionality of the scheme. Compare your results with theoretical ones.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Repeat steps 4-6 for experiment 11B.
8. Be ready to answer your instructor's questions in process of work.
9. Complete your work, dismount your schemes, clean your working place.
10. Answer your instructor's final questions, obtain your mark.
11. Ask your instructor's permission to leave.

Experiment 11A. Realize the following circuit on a breadboard. Connecting D, CLK, CD, and SD inputs to either GND or VCC based on the following table, fill in the blanks. Write ON or OFF for LEDs.



	INPUTS							OUTPUTS	
	D	CLK	CD	SD	LED1	LED2	LED3	LED4	LED5	LED6
1	0V	0V	5V	5V						
2	0V	5V	5V	5V						
3	0V	0V	5V	5V						
4	5V	0V	5V	5V						
5	5V	5V	5V	5V						
6	5V	0V	5V	5V						
7	5V	0V	0V	5V						
8	5V	0V	5V	5V						
9	5V	0V	5V	0V						
10	5V	0V	5V	5V						
11	5V	0V	0V	5V						
12	5V	0V	5V	5V						
13	5V	0V	5V	0V						
14	5V	0V	5V	5V						
15	0V	0V	5V	5V						
16	0V	0V	0V	5V						
17	0V	0V	5V	5V						
18	0V	0V	5V	0V						
19	0V	0V	5V	5V						
20	0V	5V	5V	5V						
21	0V	0V	5V	5V						
22	0V	0V	0V	5V						
23 *	0V	0V	0V	0V						
24	0V	0V	5V	0V						
25	0V	0V	5V	5V						

* be careful at that stage!

Based on the above truth table, it is a .... type flip flop, with .... is the input, ... is the clock input, ... is the output, and .... is the inverting output. SD is .... and CD is ....

Experiment 11B. Mount the D-Flip-Flop circuit implemented with NAND gates on the breadboard. Compare results with the results obtained in experiment 11A.

Conclusion.

TEST QUESTIONS

1. __________ flip-flop gives us uncertainty if set and reset inputs have value 1 at the same time.
A. RS and clocked RS B.RS or clocked RS C. D D. JK E. T

2. This is characteristic table of ______ flip-flop.

	Q (t+1)
0	0
1	1

A. RS B. Clocked RS C. D D. JK E. T

3. This is excitation table of __________ flip-flop.

Q(t)	Q (t+1)		
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

A. RS B. Clocked RS C. D D. JK E. T

4. What state sequence for Q(t+1) is correct?

J	K	Q (t+1)
0	0	
0	1	
1	0	
1	1	

A. 1, 0, Q(t), ? B. 1, 0,?, Q(t) C. Q(t), 0,1,Q´(t) D. Q(t), 0,1, 1 E. Q(t), 0,1, 0

5. Set-dominate flip-flop has got __________ input(s).
A. 1 B. 2 C. 1 or 2 D. 3 E. 2 or 3

6. D flip-flop characteristic equation is ______
A. Q(t+1)=DQ B. Q(t+1)=D+Q C. Q(t+1)=D
D. Q(t+1)=D´Q E. Q(t+1)=D´

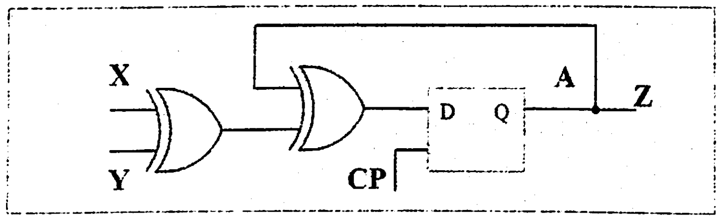
7. A state equation of the sequential circuit is
A. an expression to describe next state of the circuit
B. an expression to describe present state of the circuit
C. a Boolean function that specifies the present state conditions that make the next state equal to 1
D. a Boolean function that specifies the present state conditions that make the present state equal to 1
E. a Boolean function that specifies the next state conditions that make the present state equal to 1

8. How many options to gain state 10 will the circuit with the state table below have?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	0

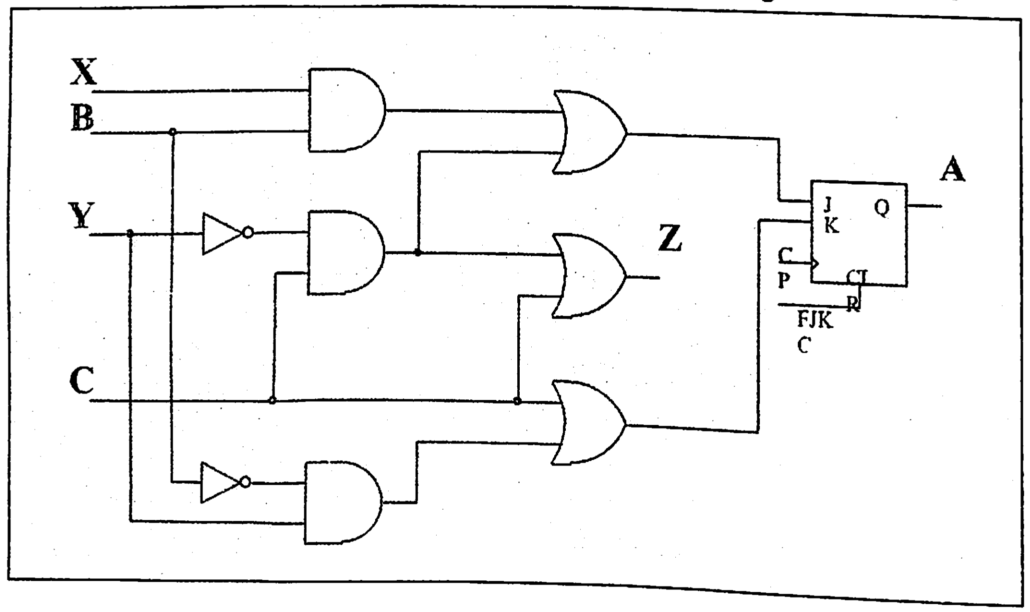
A. 1 B. 2 C. 3 D. 4 E. 5

9. What is the input equation for D flip-flop for the circuit below?



A. A+X
B. A⊕X
C. A⊕X⊕Y
D. X⊕Y
E. X⊕Y⊙A

10. For the circuit below X=1,B=1,Y=1,C=1. What will be the next state for the flip-flop?
A. set B. reset C. complement D. No change E. none



LABORATORY WORK # 12.

COUNTERS.

Aims: investigate the operations of switch tail ring counter and ripple counter.

PREPARATION TO LAB WORK.

1. Learn the information about flip-flops, registers and counters.
2. Prepare logic diagram of 4-stage switch-tail ring counter using 4 D-flip-flops, and draw it with application of Scheme Design System. This circuit will be used in experiment 12A.
3. Construct a 4-bit asynchronous ripple counter with 4 JK-flip-flops for the experiment 12B, and draw it with application of Scheme Design System.
4. Answer the question below in written form.
   4.1. What is a word-time signal?
   4.2. What is a ring counter?
   4.3. What is switch tail ring counter?
   4.4. What is ripple counter?
   4.5. What is BCD counter?
   4.6. What is the difference between synchronous and asynchronous counters?

LAB WORK PERFORMANCE.

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount the scheme of experiment 12A on the breadboard and perform it. Fill in the table.
5. Make a conclusion about functionality of the scheme. Compare your results with theoretical ones.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Repeat steps 4-6 for experiment 12B.
8. Be ready to answer your instructor's questions in process of work.
9. Complete your work, dismount your schemes, clean your working place.
10. Answer your instructor's final questions, obtain your mark.
11. Ask your instructor's permission to leave.

Experiment 12A. Construct the logic diagram of 4-stage switch-tail ring counter using 4 D-flip-flops, and mount it on the breadboard. Apply direct clear CD signal for all flip-flops. Apply active CP (clock pulse) 8 times. observing all D-flip-flops outputs (A, B, C, and E) behavior. Fill in the table.

#	CD	CP	A	B	C	E
1	0					
2	5V	↑				
3	5V	↑				
4	5V	↑				
5	5V	↑				
6	5V	↑				
7	5V	↑				
8	5V	↑				
9	5V	↑				

Experiment 12B. Construct a 4-bit asynchronous ripple counter with 4 JK-flip-flops, and mount it on the breadboard. Apply direct clear CD signal for all flip-flops. Apply active CP (clock pulse) 8 times, observing all JK-flip-flops outputs (A, B, C, and D) behavior. Fill in the table.

#	CD	CP	A	B	C	D
1	0					
2	5V	↑				
3	5V	↑				
4	5V	↑				
5	5V	↑				
6	5V	↑				
7	5V	↑				
8	5V	↑				
9	5V	↑				

Conclusion.

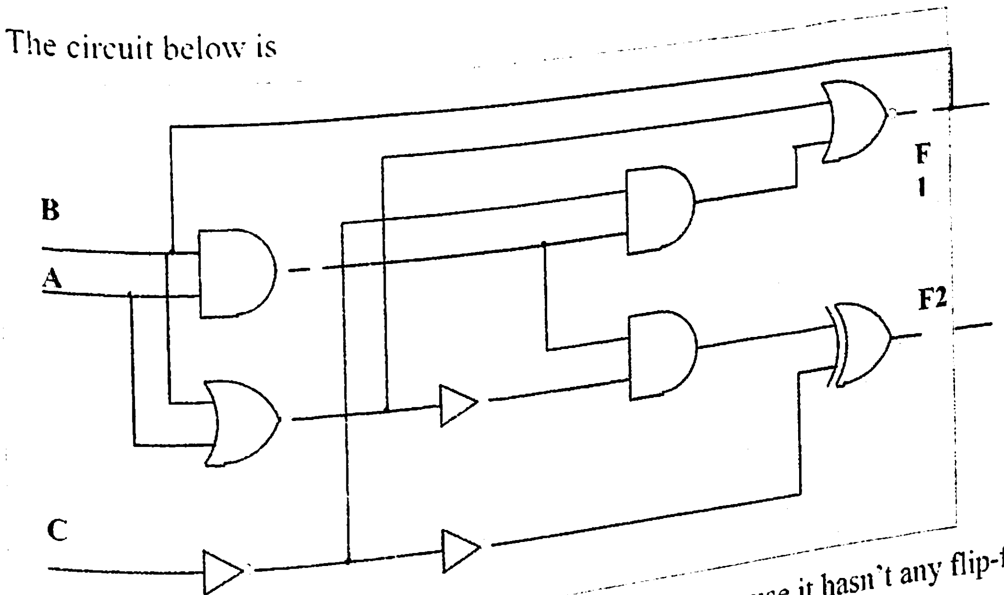
TEST QUESTIONS

1. Sequential MSI circuits may be
A. decoder, register, counter
B. multiplexer, register, counter
C. demultiplexer , register, counter
D. ROM, register, counter
E. register, counter, random-access memory

2. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the right, with the serial input being 101101. What is the content of the register after the second shift?
A. 0101 B. 1100 C. 1110 D. 1101 E. 0111

3. What statement is correct?
A. Number of different functions of two variables is equal to 8.
B. In a ripple counter, the flip-flop output transition serves as a source for triggering other flip-flops.
C. NOT is a binary operator
D. Computers may operate in a serial mode and in a parallel mode
E. Decoder with enable can be used as multiplexer

4. The circuit below is



A. combinational B. sequential C. combinational, because it hasn't any flip-flops
D. sequential, because it has a feedback path
E. sequential, because it has a feedback path between output and input

5. Sequence of 12 timing signals can be produced by Johnson counter if it has got ___ flip-flops.
A. 7 B. 6 C. 5 D. 4 E. 3

6. For the scheme of Johnson shift counter the correct sequence of states are:
A. 0000, 0001, 0010, 0011
B. 0000, 1000, 1100, 1110
C. 0000, 1000, 1001, 1010
D. 0000, 1000, 0001, 1001
E. 0000, 0001, 1000, 1001

7. For the table below the sequence for K_C is

A. X,X, X, 0,0,1 B. 0,0,1,X,X,X C. 0,1,X,0,1,X D. X,1,X,X,1,X E. 1,1,0,1,0,0

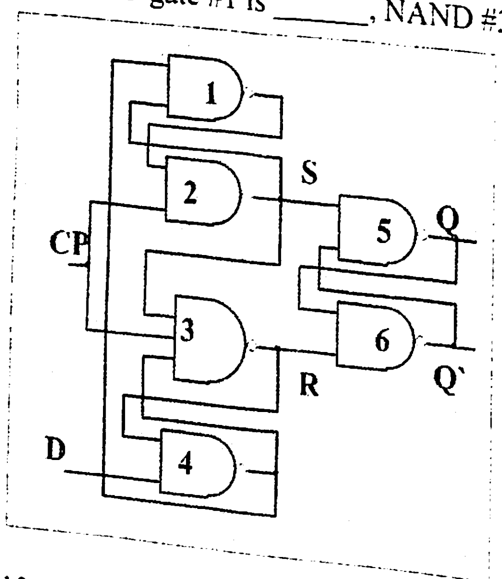
Count sequence			Flip-flop inputs					
A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	X	0	X	1	
0	0	1	0	X	1	X	X	
0	1	0	1	X	X	1	0	
1	0	0	X	0	0	X	1	
1	0	1	X	0	1	X	X	
1	1	0	X	1	X	1	0	

8. This is characteristic table of _____ flip-flop.

		Q (t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q´(t)

A. RS B. Clocked RS C. D D. JK E. T

9. For the circuit below (positive-edge-triggered D flip-flop) if CP=0 and D=0 level of signals for NAND gate #1 is ______, NAND #2 is ____, NAND #4 is ______.



A. 1, 0, 1
B. 0, 1, 1
C. 0, 1, 0
D. 1, 0, 0
E. 1, 1, 0

10. What statement defines count down operation?

A. A←A+1 B. A←A-1 C. F←A+1 D. F←A-1 E. A←A`+1

LABORATORY WORK # 13.

UP/DOWN COUNTER, DRIVER, and SEVEN SEGMENT DISPLAY.

Aims: investigate operation of the device, improving students' design and analytical skills.

PREPARATION TO LAB WORK.

1. Learn the information about counter and seven-segment drive.
2. Consider scheme of experiment 13 and prepare functionally equal scheme with application of common anode display (use Scheme Design System).
3. Fill in table #1 theoretically.
4. Configure the circuit so that it would count down. Fill in table #2.
4. Answer the questions in writing form:
A. Explain 7447 principle of operation.
B. Explain 74192 principle of operation.

LAB WORK PERFORMANCE.

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount your schemes of the experiments on the breadboard and fill in tables#1 and #2.
5. Make a conclusion about functionality of the scheme.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Be ready to answer your instructor's questions in process of work.
8. Complete your work, dismount your schemes, clean your working place.
9. Answer your instructor's final questions, obtain your mark.
10. Ask your instructor's permission to leave.

EXPERIMENT 13. Realize the following circuit on a breadboard. By pressing and releasing the switch (SW), fill in the blanks on the following table.

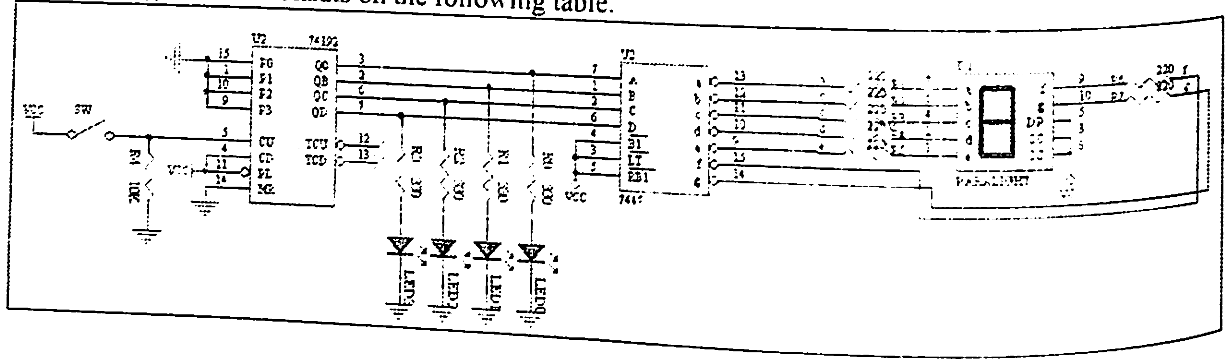


Table #1

	SW	LED3	LED2	LED1	LED0	DISPLAY
1	Press, Release					
2	Press, Release					
3	Press, Release					
4	Press, Release					
5	Press, Release					
6	Press, Release					
7	Press, Release					
8	Press, Release					
9	Press, Release					
10	Press, Release					
11	Press, Release					

Table #2

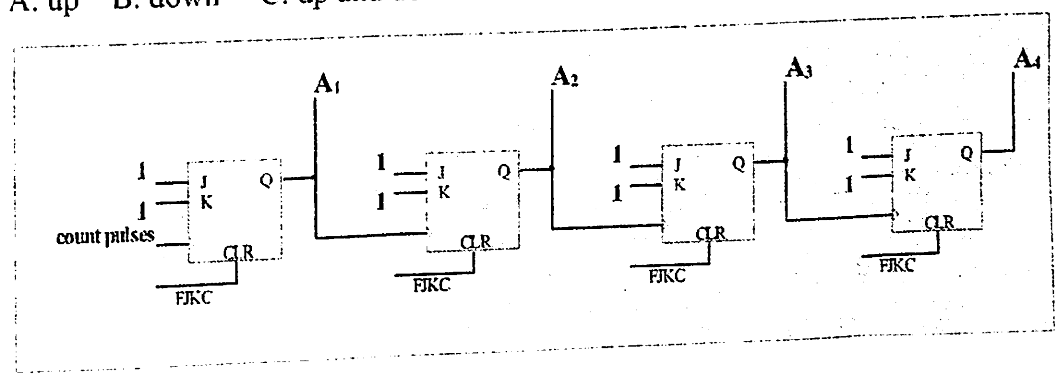
	SW	LED3	LED2	LED1	LED0	DISPLAY
1	Press, Release					
2	Press, Release					
3	Press, Release					
4	Press, Release					
5	Press, Release					
6	Press, Release					
7	Press, Release					
8	Press, Release					
9	Press, Release					
10	Press, Release					
11	Press, Release					

TEST QUESTIONS

1. If anode of each LED of the seven-segment display is connected to the 5-V supply the chip is a _____ display. It is an active-____, because it takes a _____ to illuminate a segment.
A.common-anode, LOW, LOW B. common-cathode, LOW, LOW
C. common-anode, HIGH, HIGH D. common-cathode, HIGH, HIGH
E. common-anode, HIGH, LOW

2. To have #9 on one-digit seven segment display it needs to illuminate _______ segments.
A. a, c, d, e, f, g B. a, c, d, e, f C. a, b, c, f, g D. c, d, e, f, g E. a, b, c, d, e, f

3. The circuit below can't count _______.
A. up B. down C. up and down D. None E. It is not a counter



4. 7447 is
A. 3*8 decoder B. 4-bit magnitude comparator C. priority encoder
D. D flip-flop E. BCD-to-seven-segment decoder/driver

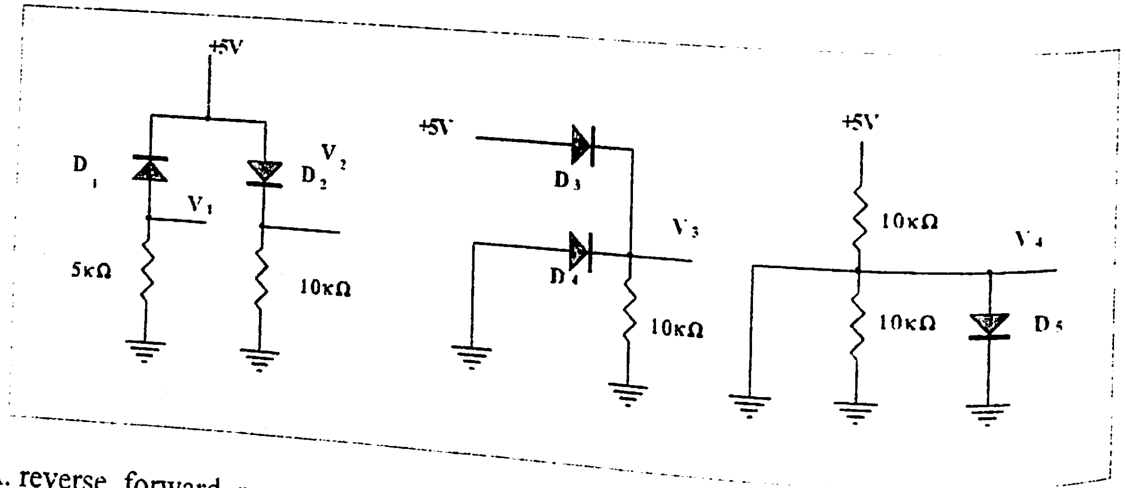
5. Master-reset input is the input
A. to initialize the states of all flip-flops in the system
B. to initialize the states of all flip-flops in the system, when clock pulse will appear C. to change the states of all flip-flops in the system
D. To clear all flip-flops asynchronously E. to set all flip-flops asynchronously

6. Enable input is the input
A. to make a device active B. to provide the normal device's operation
C. to control the circuit operation D. to make the circuit sensitive
E. to have part of the circuit active

7. 74192 is
A. up/down counter B. a BCD counter C. a BCD decade counter
D. a BCD decade up/down counter E. a register

8. The terminal count up (TCu) and terminal count down (TCd) of 74193 are normally ____.
The TCu is used to indicate that ____ count is reached.
A. HIGH, 9^{th} B.LOW, 9^{th} C. HIGH, 15^{th} D. LOW, 15 E. LOW, maximum

9. What can you say about state of diodes 1, 2, 3 in the picture?



A. reverse, forward, reverse
B. reverse, forward, forward
C. forward, reverse, forward
D. Reverse, reverse, forward
E. forward, forward, reverse

10. Parallel load input is used to change the counter ______ regardless of the conditions of the clock ______.

A. inputs, output
B. inputs, outputs
C. outputs, input
D. outputs, inputs
E. output, input

LABORATORY WORK # 14.

BIDIRECTIONAL SHIFT REGISTER.

Aims: investigate operation of the registers, improving students' design and analytical skills.

PREPARATION TO LAB WORK.

1. Learn the information about registers.
2. Draw the circuit (using Scheme Design System) for 4-bit bidirectional shift register, connecting outputs of the register to LEDs as shown in experiment 14A.
3. Fill in table theoretically.
4. Construct the circuit (using Scheme Design System) for 8-bit bidirectional shift regidter on the basis of experiment 14A. Use the resulting scheme in experiment 14B.
5. Answer the questions in writing form:
   5.1. What is register?
   5.2. What types of registers do you know?
   5.3. Explain parallel-in serial-out register.
   5.4. Explain 7447 principle of operation.
   5.5. Explain 74192 principle of operation.

LAB WORK PERFORMANCE.

1. Demonstrate presence of your home preparation for lab work to your instructor.
2. Pass test of 10 questions.
3. Get a permission to begin the work.
4. Mount your schemes of the experiment 14A on the breadboard and fill in table.
5. Make a conclusion about functionality of the scheme.
6. Demonstrate your results to your instructor. If your results are correct you may dismount your scheme, if no – find the mistake.
7. Repeat steps 4-6 for experiment 14B.
8. Be ready to answer your instructor's questions in process of work.
9. Complete your work, dismount your schemes, clean your working place.
10. Answer your instructor's final questions, obtain your mark.
11. Ask your instructor's permission to leave.

EXPERIMENT 14A. Implement the following circuit on a breadboard and fill in the blanks on the following table.

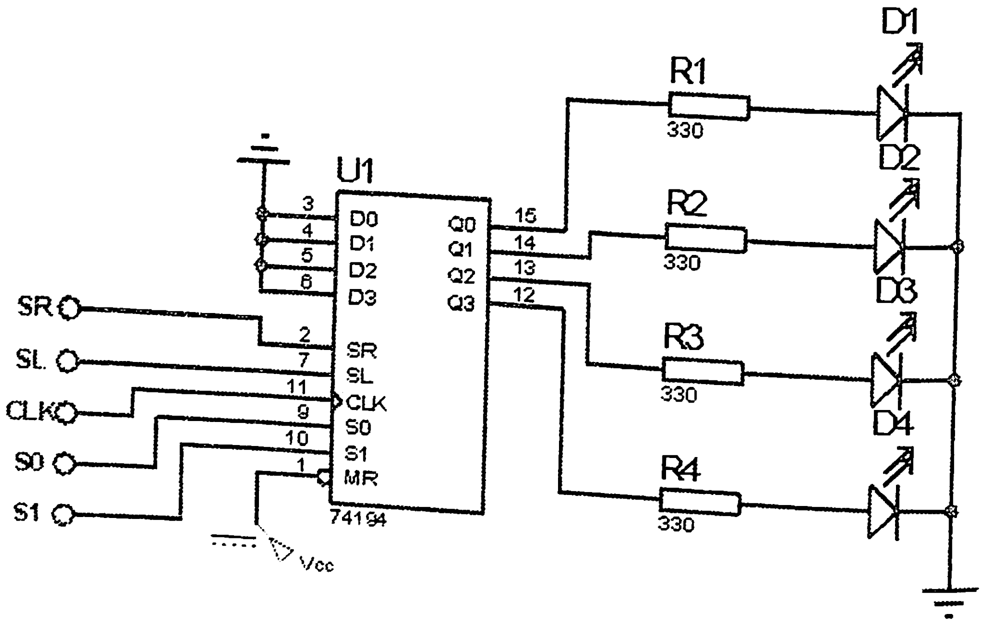


Table #1

	SR	SL	S0	S1	CLK	LED4	LED3	LED2	LED1
1	0	0	0	0	↑				
2	1	0	1	0	↑				
3	1	0	1	0	↑				
4	1	0	1	0	↑				
5	1	0	0	1	↑				
6	1	0	0	1	↑				
7	0	1	0	1	↑				
8	0	1	0	1	↑				
9	0	0	0	1	↑				
10	1	1	0	0	↑				
11	1	1	1	1	↑				

EXPERIMENT 14B. Implement the circuit of 8-bit bidirectional shift regidter using 2 4-bit bidirectional shift registers. Make appropriate connections. Configure your circuit so that it would shift the information 8 times to the left and then 8 times to th right. Compare it with the circuit in experiment 14A. Make conclusion.

Conclusion.

TEST QUESTIONS

1. The transfer a new information into register is called _____ of register.
A. triggering B. Loading C. Set D. Reset E. none of above mentioned

2. Loading of register is done in parallel if
A. the bits of the register are loaded simultaneously
B. all the bits of the register are loaded simultaneously
C. all the bits of the register are loaded simultaneously with a clock pulse
D. all the bits of the register are loaded simultaneously with a single clock pulse
E. the bits of the register are loaded simultaneously with a single clock pulse

3. How many control signals has bidirectional shift register with parallel load got?
A. 2 B. 3 C.4 D.5 E.6

4. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the right, with the serial input being 101101. What is the content of the register after the first shift?
A. 0101 B. 1100 C. 1110 D. 1101 E. 1010

5. What types of operation bidirectional shift register with parallel load has?
A. shift right, parallel load B. shift left, parallel load
C. shift right, shift left, parallel load D. Complement, no change
E. shift right, shift left, parallel load, no change

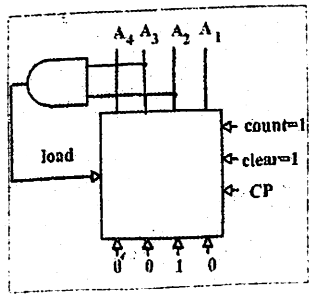
6. Feedback shift register is such type of register, when
A. each flip-flop transfers its content to the next flip-flop
B. each flip-flop transfers its content to the next flip-flop, when a clock pulse occurs
C. each flip-flop transfers its content to the next flip-flop, when a clock pulse occurs, but the next state of the first flip-flop(for MSD) is some function of the present state of other flip-flops
D. each flip-flop transfers its content to the next flip-flop, when a clock pulse occurs, but the next state of the first flip-flop(for LSD) is some function of the present state of other flip-flops
E. each flip-flop transfers its content to the next flip-flop, when a clock pulse occurs, but the next state of the last flip-flop(for LSD) is some function of the present state of other flip-flops

7. If Johnson counter has got 3 flip-flops, we can have sequence of _____ timing signals.
A. 3 B. 4 C. 5 D. 6 E.9

8. For what purpose is buffer used?
A. to reduce loading of the device to which the buffer is connected C. to decrease propagation delay
B. to improve characteristics of the circuit E. all aforementioned answers are wrong
D. to increase propagation delay

9. A flip-flop has a 10-ns delay from the time its CP input goes from 1 to 0 to the time the output is complemented. What is the maximum frequency the counter can operate at reliably?
A. 5 MHz B. 6.25 MHz C. 8.33 MHz D. 10 MHz E. 12.5 MHz

10. The circuit below is a mod-_____ counter.
A. 1 B. 2 C. 3 D. 4 E. 5



LITERATURE

1. M. Morris Mano. Digital Logic and Computer Design.1999
2. William Kleitz. Digital Electronics. A Practical Approach. Forth Edition. Prentice- Hall International, Inc. 1996
3. Larissa A. Kiziyeva. Digital Design. Test Questions. SDU.Almaty, 2002
4. Dr. Melik Şah Ertugrul, Larissa A. Kiziyeva. Digital Design.Lab works' description. SDU. Almaty, 2005
5. M.Morris Mano, Michael D. Çiletti. Digital Design (4^{th} eddition). Prentice- Hall of India 2008
6. Robert Boylestad, Louis Nashelsky. Electronic Devices and circuit theory. PRENTICE HALL 2008