SÜLEYMAN DEMIREL UNIVERSITY

Faculty of Engineering

Department of Natural Sciences, Mathematics and Informatics

DIGITAL DESIGN

TEST QUESTIONS

LARISSA A. KIZIYEVA

Almaty o 2002

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Larissa A. Kiziyeva

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PREFACE

Digital Design is one of the basic courses for computer engineers. Then students study special courses on the basis of Digital Design one. Thus, good knowledge of the course is a warranty of a successful study in whole.

Test questions are prepared on the basis of material of eight chapters of M. Morris Mano manual "Digital Logic and Computer Design". They cover such topics as "Binary Systems", " Boolean Algebra and Logic Gates", " Simplification of Boolean Functions", " Combinational Logic", " Combinational Logic with MSI and LSI"," Sequential Logic", " Registers, Counters, and the Memory Unit", " Register Transfer Logic". Test questions are prepare such a way to cover the course in whole. As a base of the test preparation methodic Bloom's taxonomy is used. It allows us to control the test questions'-level of complexity. It is known that Bloom's taxonomy provides a useful structure in which to categorize test questions, since professor will characteristically ask questions within particular levels. Bloom proposes such levels of students' competence: 1) knowledge; 2) comprehension; 3) application; 4) analysis; 5) synthesis; 6) evaluation.

In our case the main part of test questions is of levels 2, 3, and 4. There are few test questions of level 1, because on average the level of Suleyman Demirel University (SDU) students' knowledge is enough high. There are few test questions of level 5 and 6 too, because according to methodic of SDU students' knowledge checking, the tests are method only preliminary evaluation of students' knowledge and skills. Tests are used only as indicators for students and for instructor. A student can evaluate the level of his knowledge and make a decision if he wants to improve his knowledge on the subject or it is enough for him to obtain a minimum positive mark as a result of the test passage. From another side, an instructor makes a selection of students according to different criteria on the basis of the tests' results. Instructor defines the best students for creative work with them and the worst students for correction of their knowledge. Students who obtained definite number of points on the test have got a right to take part in a creative exam. During the exam they have got the tasks of levels 5 and 6 according to Bloom's taxonomy. But they must demonstrate the ways of the tasks' solution completely, show the results obtained, analyze, evaluate them, make a conclusion, they must enunciate all statements themselves.

The test questions are prepared such a way, that correspondent choice may be done at any stage of the course. It gives a possibility to carry out check of the students' knowledge any moment. SDU authority can carry out it without presence of the instructor because the list if correct answers is prepared.

The test questions give possibilities to students to concentrate their efforts in the important directions. According to the test questions' content they can judge about the level of requests to pass the exam and what is more important in the subject. Publishing of the test questions doesn't mean that they will be for exam exactly. They can be used only for orientation, but during the exam such changes will be done: for number base conversion the data are different, the scheme for analysis is different too and so on. But if a student can answer these published test questions, he will be able to any questions of the same levels.

The test questions will be very useful for students and any persons who are interested in their English improving, because in process of the test questions' preparation terms, typical structures of sentences of scientific English are used.

Author

Digital Design
Test Questions.

1. Obtain the result of binary division: 11011101:00010001

(A) 1101 B. 1010 C. 1001 D. 10101 E. 11101

2. A basic operation in digital system is

A. Addition B. Multiplication C. Conversion D. Complementing
(E) Inter-register transfer operation

3. The register's content is:

1	0	0	0	0	1	0	0	0	1	1	0

In BCD it represents:

(A) 846 B.946 C. 856 D. 956 E. 945

4. The truth table for AND gate is:

(A)

x	y	F
0	0	0
0	1	0
1	0	0
1	1	1

B

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

C

x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

D

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

E

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

5. The truth table for XOR gate is:

A

x	y	F
0	0	0
0	1	0
1	0	0
1	1	1

B

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

C

x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

D

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

(E)

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

6. The truth table for NAND gate is:

A

x	y	F
0	0	0
0	1	0
1	0	0
1	1	1

B

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

(C)

x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

D

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

E

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

7. The truth table for OR gate is:

A

x	y	F
0	0	0
0	1	0
1	0	0
1	1	1

(B)

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

C

x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

D

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

E

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

8. The truth table for NOR gate is:

A

x	y	F
0	0	0
0	1	0
1	0	0
1	1	1

B

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

C

x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

(D)

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

E

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

9. The truth table for XNOR gate is:

(A)

x	y	F
0	0	1
0	1	0
1	0	0
1	1	1

B

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

C

x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

D

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

E

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

10. The content of register when we enter 249 in BCD is:

(A)	0	0	1	0	0	1	0	0	1	0	0	1
B	0	0	1	0	0	1	0	0	1	0	0	0
C	0	1	0	0	0	0	1	0	1	0	0	1
D	0	0	1	1	0	1	0	0	1	0	0	0
E	0	0	1	0	0	0	1	1	1	0	0	1

11. Convert $(127.4)_8$ to decimal:

A.74.6 B. 67.5 C. 84.5 D. 87.6 (E.) 87.5

12. Convert $(B65F)_{16}$ to decimal:

A. 35576 (B.) 46687 C. 35676 D. 46587 E. 45372

13. Convert $(0101100011010 11.111100000110)_2$ to octal:
(A) 26153.7406 B. 27153.7406 C. 26351.7206 D. 26143.6406 E. 26153.7206

14. Convert $(0010110001101011)_2$ to hex:
A. 3B6C B. 3C6B C. 2C5B D. 2B6C (E) 2C6B

15. Convert $(673)_8$ to binary:

A. 110101011 B. 111110011 (C.) 110111011 D. 110111100 E. 110111010

16. Convert $(3A6)_{16}$ to binary:

(A.) 1110100110 B. 1010100110 C. 1100100110 D. 1110010110 E. 1110101010

17. Convert decimal 369 to binary, octal, and hex:

A. 101110001, 461, 171
B. 101110001, 269, 171
C. 100110001, 561, 271
D. 100110001, 461, 271
(E.) 101110001,561,171

18. Convert binary 110101 to decimal, octal, and hex:

A. 53, 56, 45 B. 43, 65, 35 C. 53, 65, 35 D. 43, 56, 45 E. 53, 65, 25

19. Convert octal 206 to binary, decimal, and hex:

A. 10000110, 134,68
B. 10000110, 134, 86
C. 10000110, 234, 86
D. 10010110, 134, 68
E. 11000110, 234, 66

20. Convert hex F01 to binary, octal, and decimal:

A. 110100000000, 6351, 2821
B. 111100000001, 6351, 3841
C. 110100000001, 7203, 2821
D. 111100000001, 7401, 3841
E. 110100000010, 6351, 2841

21. A small-scale integration (SSI) device contains _____ gates in a single chip.
A. thousands of B. From10 to 1000 C. More than 100
D. From 10 to 100 (E.) less than 10

22. A medium-scale integration (MSI) device contains _____ gates in a single chip.

A. thousands of B. From10 to 1000 C. More than 100
(D.) From 10 to 100 E. less than 10

23. A large-scale integration (LSI) device contains _____ gates in a single chip.
A. thousands of B. From10 to 1000 (C.) More than 100
D. From 10 to 100 E. less than 10

24. A very-large-scale integration (VLSI) device contains _____ gates in a single chip.
(A.) thousands of B. From10 to 1000 C. More than 100
D. From 10 to 100 E. less than 10

25. Binary combination 01011 can be expressed as

(A.) A'BC'DE B. A'B'C'DE C. ABC'DE D. A'BCD'E E. A'B'CDE

26 Binary combination of term WX'YZ' is:

A. 0101 B. 1101 (C.) 1010 D. 0111 E. 1011

27. Binary combination 0110 can be expressed as

A. W+ X+Y+Z' B. W+X+Y+Z C. W+X'+Y+Z
(D.) W+X'+Y'+Z E. W'+X'+Y+Z

28 Binary combination of term X'+Y'+Z is:

A 001 (B) 110 C. 101 D. 010 D 011

29. How many functions of 2 variables do you know?

A. 4 B. 8 (C.) 16 D. 24 E. 32

30. The function F = (0,1, 3, 4, 7). Expression of the function's complement is:

A. F' = (5, 6) (B.) F' = (2, 5, 6) C. F' = (0, 1, 3, 4, 7)
D. F' = (0, 1, 5, 6) E. F' = (0, 2, 5, 6)

31. Expression of the function F= (0, 3, 6, 7) in product of m axterms form is:

A. F= (1, 2, 3, 5) B. F= (4, 5, 6, 7) C. F= (1, 2, 6, 7)
(D.) F= (1, 2, 4, 5) E. F= (1, 2, 5, 6)

32. Expression of the function F= (1, 2, 4) in sum of minterms form is:

A. F= (3, 5, 6, 7) B.F= (0, 3, 5, 6) C. F= (0, 3, 5, 7)
D. F= (0, 2, 5, 6) (E) F= (0, 3, 5, 6, 7)

33. Express the function F(X,Y,Z), using the truth table:

X	0	0	0	0	1	1	1	1
Y	0	0	1	1	0	0	1	1
Z	0	1	0	1	0	1	0	1
F	1	0	0	1	0	0	0	1

A. X'Y'Z'+X'YZ+XYZ B. X'Y'Z+X'YZ+XYZ (C.) X'Y'Z'+YZ
D. X'Y'Z+XY'Z+XYZ E. X'Y'Z'+X'Y'Z+X'YZ

34. Number of functions of n variables can be determined according to the formula

(A) 2^{2^n} B. 2^{2n} C. 2^n D. 2^{3^n} E. 2^{3n}

35. XY′+X′Y is algebraic expression of _____ function.
(A) XOR B. XNOR C. NOR D. NAND E. AND

36. (XY)′ is algebraic expression of _____ function.

A. XOR B. XNOR C. NOR (D) NAND E. AND

37. XY is algebraic expression of _____ function.

A. XOR B. XNOR C. NOR D. NAND (E) AND

38. (X+ Y)′ is algebraic expression of _____ function.

A. XOR B. XNOR (C) NOR D. NAND E. AND

39. XY+X′Y′ is algebraic expression of _____ function.

A. XOR (B) XNOR C. NOR D. NAND E. AND

40. The basic circuit in each digital logic family is_____ gate(s):

A. AND or OR B. Only NAND C. Only NOR
D. AND and OR (E) NAND or NOR

41. If the system requires high-speed operations it would be better to use chips of _____ logic family.

A. TTL (B) ECL C. MOS D. CMOS E. I^2L

42. If the system requires low power consumption it would be better to use chips of _____ logic family.

A. TTL B. ECL C. MOS (D) CMOS E. I^2L

43. If the system requires high component density it would be better to use chips of _____ logic family.

A. TTL B. ECL C. MOS D. CMOS (E) I^2L and MOS

44.7400 is IC of _____ logic family.

(A) TTL B. ECL C. MOS D. CMOS E. I^2L

45. 4000 is IC of _____ logic family.

A. TTL B. ECL C. MOS (D) CMOS E. I^2L

46. Typical voltage for IC TTL logic family for positive logic is for HIGH -_____V, for LOW - _____V.

A. 0.2, 3.5 (B) 3.5, 0.2 C. 5, 0 D. 0, 5 E. 0, 3.5

47. Typical voltage for IC TTL logic family for negative logic is for HIGH -_____V, for LOW - _____V.

(A) 0.2, 3.5 B. 3.5, 0.2 C. 5, 0 D. 0, 5 E. 0, 3.5

48. 14 pin TTL SSI chip can contain _____ 2 input XOR gates.

A. 1 B. 2 C. 3 (D) 4 E. 5

49. 14 pin TTL SSI chip can contain _____ 3 input AND gates.

A. 1 B. 2 (C) 3 D. 4 E. 5

50. 14 pin TTL SSI chip can contain _____ 4 input NAND gates.

A. 1 (B) 2 C. 3 D. 4 E. 5

51. 14 pin TTL SSI chip can contain _____ 5 input NOR gates.

A. 1 (B) 2 C. 3 D. 4 E. 5

52. A encoder is a combinational circuit that

A. converts binary information from n input lines to a maximum of 2^n unique output lines
(B) has 2^n (or less) unique input lines and n output lines
C. selects binary information from one of many input lines and direct it to a single output line
D. receives information on a single line and transmits this information on one of 2^n possible output lines
E. converts binary information from n input lines to m output lines

53. _____ flip-flop gives us uncertainty if set and reset inputs have value 1 at the same time.
(A) RS and clocked RS B.RS or clocked RS C. D D. JK E. T

54. _____ flip-flop hasn't undetermined states and has 2 inputs, including CP
A. RS B. clocked RS C. set-dominate RS D. JK (E) T

55. Master-slave flip-flop consists of _____ flip-flop(s).

A. 1 (B) 2 C.1 or 2 D. 3 E. 2 or 3

56. A synchronous sequential circuit is a system whose behavior

A. depends upon the order in which its input signals change
B. depends upon the order in which its input signals change and can be affected at any instant of time
C. can be defined from the knowledge of its signals
D. can be defined from the knowledge of its signals at discrete instants of time
E. can be defined by sequence of pulses

57. Power dissipation is

A. the power consumed by the gate
B. the power consumed by the gate, which must be available from the power supply
C. the power consumed by the gate, which may be available from the power supply
D. the power emitted by the gate
E. the power emitted by the gate, which may be available for the gates of the next level

58. A register is
A. a group of storage cells suitable for holding information
B. a group of storage cells suitable for holding binary information
C. a group of binary cells suitable for holding information
D. a group of binary storage cells suitable for holding binary information
E. a group of binary cells suitable for processing information

59. A full subtractor is a _____ circuit, that performs a subtraction _____ bits, taking into account that a _____ may have been borrowed by a _____ significant stage.

A. sequential; of three; 1; higher
B. sequential; between two; carry; higher
C. combinational; between two; 1; higher
D. combinational; of three; carry; lower
E. combinational; between two; 1; lower

60. A read-only memory (ROM) is a device that includes _____ within a single IC package

A. the decoders and the OR gates
B. the decoder and the OR gates
C. the decoders and the OR gate
D. the decoders and the AND gates
E. the decoders and the NAND gates

61. A decoder is a combinational circuit that

A. converts binary information from n input lines to a maximum of 2^n unique output lines
B. has 2^n (or less) unique input lines and n output lines
C. selects binary information from one of many input lines and direct it to a single output line
D. receives information on a single line and transmits this information on one of 2^n possible output lines
E. converts binary information from n input lines to m output lines

62. Serial binary adder consists of

A. n full adders, connected in cascade, where n-number of digits for addition
B. n half adders, connected in cascade, where n-number of digits for addition
C. n full adders and a storage device, where n-number of digits for addition
D. n half adders and a storage device, where n-number of digits for addition
E. one full adder and a storage device

63. _____ flip-flop hasn't undetermined states and has 3 inputs, including CP

A. RS B.clocked RS C. D D. JK E. T

64. Noise margin is
A. the limit of a noise voltage
B. the limit of a noise voltage, which may be present without impairing the operation of the circuit
C. the limit of a noise voltage, which may be present without impairing the proper operation of the circuit
D. the limit of voltage, which may be present without impairing the operation of the circuit
E. the limit of voltage, which may be present without impairing the proper operation of the circuit

65. Counter is

A. a circuit that goes through a prescribed sequence of states
B. a sequential circuit that goes through a prescribed sequence of states
C. a circuit that goes through a prescribed sequence of states upon the application of pulses
D. a circuit that goes through a prescribed sequence of states upon the application of input pulses
E. a sequential circuit that goes through a prescribed sequence of states upon the application of input pulses

66. A half-subtractor is a _____ circuit, that subtracts _____ bits and produces their difference.
A.sequential; three
B. sequential; two
C. combinational; two
D. combinational; three
E. sequential or combinational; three

67. Chip is

A. integrated circuit
B. integrated circuit, containing transistors, diodes, resistors, capacitors
C. circuit, containing transistors, diodes, resistors, capacitors
D. integrated circuit, containing photo diodes and opto couples
E. integrated circuit, containing transistors and diodes

68. The MOSFET can have such regimes of operation:

A. cutoff and saturation
B. forward bias and reverse bias
C. depletion and enhancement mode
D. with p-channel and n-channel
E. with induced channel and internal channel

69. Propagation delay is

A. the average transition delay time for the signal to propagate from input to output when the signals change in value
B. the average transition delay time for the signal to propagate from input to output
C. the transition delay time for the signal to propagate from input to output
D. the transition delay time for the signal to propagate from input to output when the signals change in value
E. the average transition delay time for the signal to propagate from input of one gate to input of the next gate

70. A demultiplexer is a combinational circuit that

A. converts binary information from n input lines to a maximum of 2^n unique output lines
B. has 2^n (or less) unique input lines and n output lines
C. selects binary information from one of many input lines and direct it to a single output line
D. receives information on a single line and transmits this information on one of 2^n possible output lines
E. converts binary information from n input lines to m output lines

71. Each active input signal can switch _____ flip-flop in complement state.
A. RS B. clocked RS C. D D. JK E. T

72. A asynchronous sequential circuit is a system whose behavior

A. depends upon the order in which its input signals change
B. depends upon the order in which its input signals change and can be affected at any instant of time
C. can be defined from the knowledge of its signals
D. can be defined from the knowledge of its signals at discrete instants of time
E. can be defined by sequence of pulses.

73. Master-clock generator is

A. a timing device
B. a timing device which generates a periodic pulses
C. a timing device which generates a periodic train of pulses
D. a timing device which generates a periodic train of clock pulses
E. a timing device which generates a train of clock pulses

74. A shift register is a register which

A. capable of shifting its binary information
B. capable of shifting its binary information to the right
C. capable of shifting its binary information to the left
D. capable of shifting its binary information either to the right or to the left
E. capable of shifting its binary information either to the right and to the left

75. A bidirectional shift register is a register which

A. capable of shifting its binary information
B. capable of shifting its binary information to the right
C. capable of shifting its binary information to the left
D. capable of shifting its binary information either to the right or to the left
E. capable of shifting its binary information either to the right and to the left

76. Full adder forms _____, but half-adder forms _____.

A. the sum of two bits, ... the sum of two bits and a previous carry.
B. the sum of two bits, ... the sum of two bits and a carry
C. the sum of two bits, ... the sum of two bits and a present carry
D. the sum of two bits and a carry,... the sum of two bits
E. the sum of two bits and a previous carry, ... the sum of two bits

77. Priority encoder establishes _____ to ensure that only the highest –priority input line is encoded.
A. a priority B. a line priority C. An input priority
D. an output priority E. a general priority

78. The logic diagram of full-adder consists of
A. 2 Ex-OR gates and 2 OR-gates
B. 2 Ex-OR gates and 1 OR-gate
C. 2 Ex-OR gates, 1 OR-gate, and 2 AND-gates
D. 2 Ex-OR gates, 1 OR-gate, and 1 AND-gate
E. 1 Ex-OR gate, 1 OR-gate, and 2 AND-gates

79. A multiplexer is a combinational circuit that
A. converts binary information from n input lines to a maximum of 2^n unique output lines
B. has 2^n (or less) unique input lines and n output lines
C. selects binary information from one of many input lines and direct it to a single output line
D. receives information on a single line and transmits this information on one of 2^n possible output lines
E. converts binary information from n input lines to m output lines

80. Parallel binary adder consists of

A. n full adders, connected in cascade, where n-number of digits for addition
B. n half adders, connected in cascade, where n-number of digits for addition
C. n full adders and a storage device, where n-number of digits for addition
D. n half adders and a storage device, where n-number of digits for addition
E. one full adder and a storage device

81. Read-only memory (ROM) may be

A. programmed by mask programming
B. programmable ROM
C. erasable programmable ROM
D. electrically alterable ROM
E. programmed by mask programming and programmable

82. If the next state of the flip-flop is the same as the state of input and is independent on the value of its present state, this is _____ flip-flop.

A. RS B.clocked RS C. D D. JK E. T

83. Strobe is
A. enable input of decoder
B. disable input of decoder
C. enable input of multiplexer
D. disable input of demultiplexer
E. disable input of multiplexer

84. Fan-out specifies

A. the number of loads that the output of the gate can drive without impairment of its operation
B. the number of standard loads that the output of the gate can drive without impairment of its operation
C. the number of loads that the output of the gate can drive without impairment of its normal operation
D. the number of standard loads that the output of the gate can drive without impairment of its normal operation
E. the number of loads that the input of the gate can drive without impairment of its operation

85. Positive-logic NOR gate is the same as negative-logic _____ gate.
A. OR B. NAND C. AND D. XOR E. XNOR

86. Positive-logic NAND gate is the same as negative-logic _____ gate.

A. OR B. NOR C. AND D. XOR E. XNOR

87. Positive-logic OR gate is the same as negative-logic _____ gate.

A. NOR B. NAND C. AND D. XOR E. XNOR

88. Positive-logic AND gate is the same as negative-logic _____ gate.

A. OR B. NAND C. NOR D. XOR E. XNOR

89. A majority gate is

A. a circuit whose output is equal to 1 if the majority of the inputs are 1's, otherwise the output is 0
B. a digital circuit whose output is equal to 1 if the majority of the inputs are 1's, otherwise the output is 0
C. a circuit whose output is equal to 1 if the majority of the inputs are 1's
D. a digital circuit whose output is equal to 1 if the majority of the inputs are 1's
E. a digital circuit whose output is equal to 1 if the majority of the inputs are 0's, otherwise the output is equal to 1

90. A 4-input majority gate has got a truth table:

A.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

B.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

C.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

D.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

E.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

91.A majority gate for 5 variables must have output 1 if number of 1's for inputs is equal to

A. 3 B. 3 and 4 C. 3, 4, or 5 D. 4 and 5 E. 5

92. A majority gate for 4 variables must have output 1 if number of 1's for inputs is equal to
A. 2 B. 2 and 3 C. 3 or 4 D. 4 E. 2, 3, and 4

93. A majority gate for 6 variables must have output 1 if number of 1's for inputs is equal to
A. 3 B. 3 and 4 C. 3, 4, 5 or 6 D. 4 , 5 or 6 E. 6

94. Simplification of the Boolean function F= (A+B)'(A'+B')' to a minimum number of literals is:

A. AB B. 0 C. A+B D. A E. B

95. Simplification of the function F(A,B,C,D) according to the map is:

1	1		1
			1
1	1		1

A. B′D+B′C′+A′CD′ B. B′D+B′C′+A′CD C. B′D+B′C′+ACD′
D. B′D+B′C′+A′C′D′ E. B′D′+B′C′+A′CD′

96. Simplification of the function F(A,B,C,D) according to the map is:

1	1		1
			1
1	1		1

A. (C′+D)(A+B′)(C′+B) B. (C′+D)(A+B′)(C′+B′) C. (C′+D)(A+B′)(C′+B′)
D. (C′+D′)(A′+B′)(C+B′) E. (C′+D′)(A′+B)(C+B′)

97.Complement of the function F(A,B,C,D) according to the map is:

1	1		1
			1
1	1		1

A. CD+AB+ BC′ B. C′D+AB+ BC′ C. CD+AB+ B′C
D. C′D′+AB′+B′C E. C′D′+AB′++A′BC′

98. Simplification of the function F(A,B,C,D) according to the map is:

1	1		1
X		X	1
X			X
1	1		1

A. B′D′+B′C B. B′D+B′C′ C. D′+B′C′ D. D+B′C′ E. B′D′+B′C′

99. Complement of the function F(A,B,C,D) according to the map is:

1	1		1
			X
1	1	X	1

A. B+CD′ B. B′+C′D C. B′+CD D. B+C′D′ E. B+CD

100. Simplification of the function F(A,B,C,D) according to the map is:

1	1		X
			X
1	1	X	1

A. B(A+C′) B. B′(A+C′) C. B′(A′+C′) D. B′(A+D′) E. B′(A+D)

101. Applying tabulation method we can match _____ with 0010:

A. 1010 B. 0111 C. 1110 D. 0101 E. 1011

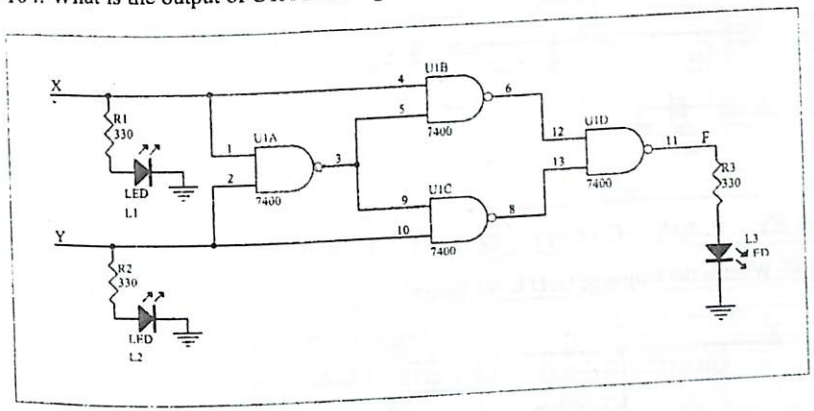
102. What were don't care conditions d(A,B,C,D) to have the function F(A,B,C,D) = AB′C′ +A′B′D′+A′CD′+A′BC′D as F(A,B,C,D)=A′B+A′D′+B′C′ ?

A. (1,3,4,7) B. (1,3,15) C. (1,7,15) D. (3,7,14,15) E. (1,4,7)

103. Canonical form of a function's representation can give us its _____ level implementation.

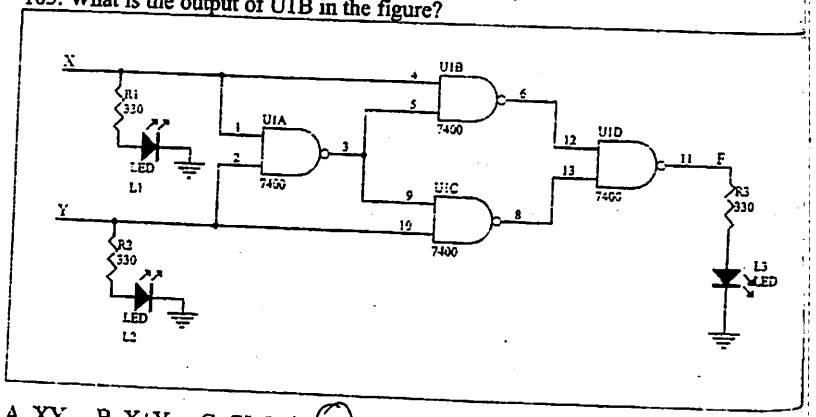
A. 1 B. 2 C. 1 or 2 D. 3 E. 2 or 3

104. What is the output of U1A in the figure?



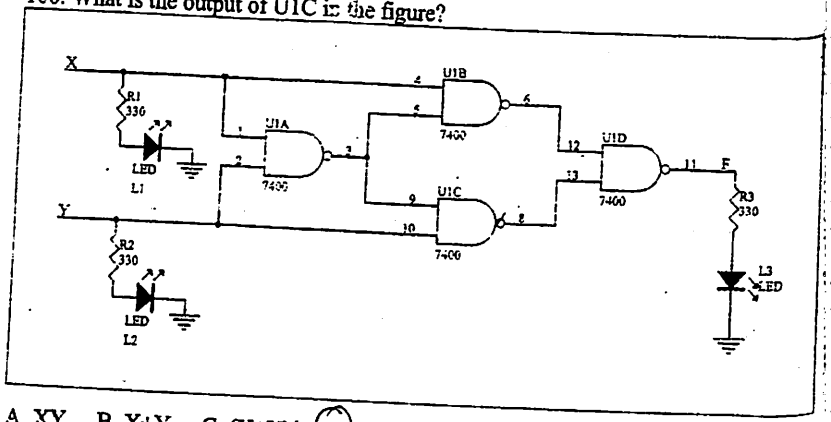
A. XY B. X+Y C. (X+Y)′ D. X′+Y′ E. (XY)′

105. What is the output of U1B in the figure?



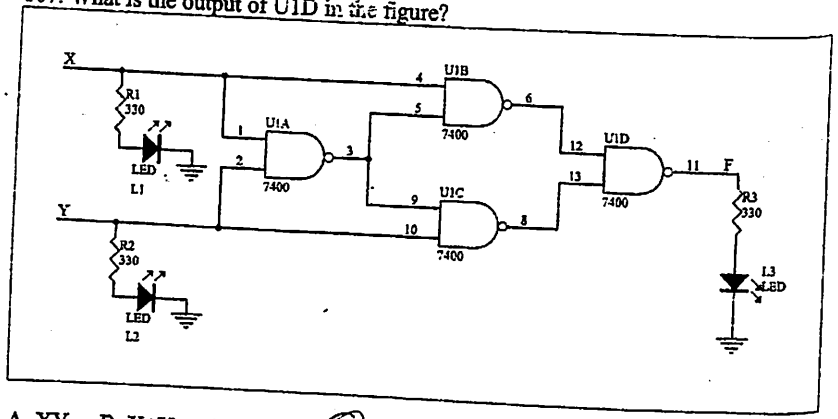
A. XY B. X+Y C. (X+Y)′ (D) X′+XY E. (XY)′

106. What is the output of U1C in the figure?



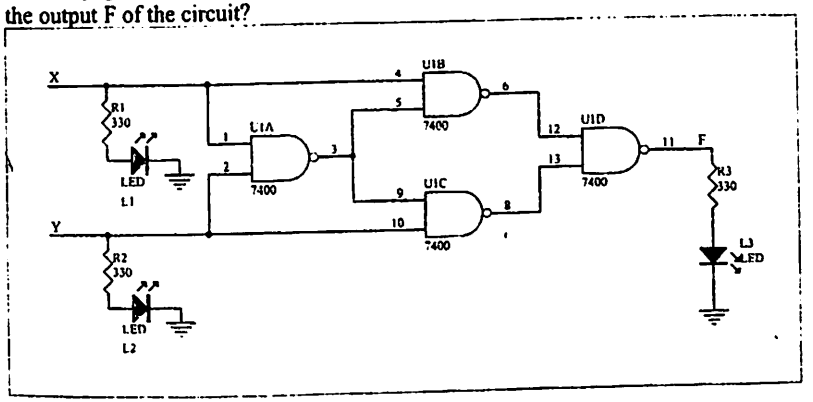
A. XY B. X+Y C. (X+Y)′ (D) XY+Y′ E. (XY)′

107. What is the output of U1D in the figure?



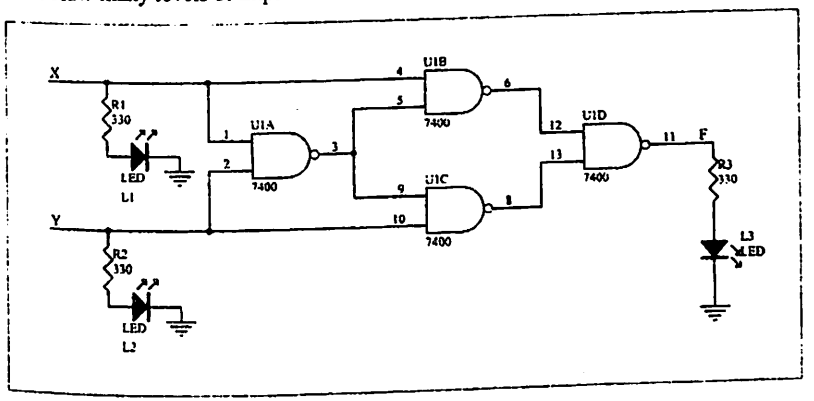
A. XY B. X+Y C. (X+Y)′ (D) XY′+X′Y E. (XY)′

108. Propagation delay of NAND gate in the figure is 10ns. What is propagation delay of the output F of the circuit?



A. 10ns B. 20ns (C) 30ns D. 40ns E. 50ns

109. How many levels of implementation the scheme in the figure has?



A. 1 B. 2 (C) 3 D. 4 E. 5

110. Which function is in its standard form?

A. A+B(C+D) (B) A+BC C. (AB+ CD)(A+C) D. (A+B)(CD+AB′)
E. (A′B′+CD)(AB′+C′D)

111. Convert sum of minterms to product of maxterms (3 variables): (0,1,3,7)
(A) (2,4,5,6) B. (0,1,3,7) C. (0,2,4,8) D. (2,4,5,6,8) E. (0,1,3,7,8)

112. We have got the map:

A \ B	1	X	X
X	1	1	X

C

Simplified function is equal to:
A. C B. A+C (C) 1 D. A +AC E. B+ B C

113. Decimal equivalent of the binary number of 11 is:

(A) $1*2^1+1*2^0$ B. $1*2^2+1*2^1$ C. $1*2^2+1*2^0$ D. $1*2^1+1*2^{-1}$ E. $1*2^0+1*2^{-1}$

114. Multiplication of two binary numbers (11 and 11) equals to:

A. 1010 B. 0111 C. 1101 D. 1011 (E.) 1001

115. 1's complement of binary number of 10011 is equal to:

(A.) 01100 B. 01101 C. 10010 D. 01110 E. 10001

116. A magnitude comparator is a _____ circuit, which determines whether

(A.) Combinational; A>B, A B, or A<B.
B. Combinational; A>B, A B, and A<B.
C. Sequential; A>B, A B, or A<B.
D. Sequential; A>B, A B, and A<B.
E. Combinational or sequential; A>B, A B, or A<B.

117. If we want to have 4*16 decoder we may construct it with:

A. multiplexer and 3*8 decoder
B. two 2*4 decoders
C. three 2*4 decoders
(D.) two 3*8 decoders
E. two 2*4 decoders and two 3*8 decoders

118. What is the best circuit for implementation of such one, which has several inputs, a lot of outputs and a lot of don't-care conditions?

A. ROM (B.) PLA C. Decoder D. Encoder E. multiplexer

119. We have got function F=(A B+CD). Only normal variables are available. To implement it we must use such gates for one scheme:

(A.) 2 NOT gates, 2 AND gates, and OR gate
B. 1 NOT gate, 2 AND gates, and OR gate
C. 2 NOT gates, 2 AND gates, and OR gate
D. 3 NOT gates, 2 NAND gates, and OR gate
E. 2 NOT gates, 2 NAND gates, and OR gate

120. A 2-bit by 2-bit binary multiplier consists of:

A. 4 AND gates B. full-adder and 4 AND gates
C. full- adder, half-adder, and 4 AND gates
D. 2 full- adders and 4 AND gates (E.) 2 half-adders and 4 AND gates

121. What statement is wrong?

A. X+X'=1 B.X+0=X C. X*1=X D. X*X'=0 (E.) X+1=X

122. What statement is wrong?

A. X+X'=1 B.X+0=X C. X*1=X (D.) X*X'=1 E.X+1=1

123. What statement is wrong?

A. X+X'=1 B.X+0=X C. X*1=X D. X*X'=0 (E.) X+X=1

124. What statement is wrong?

(A.) X+X'=0 B.X+0=X C. X*1=X D. X*X'=0 E.X+1=1

125. What statement is wrong?

A. (X+Y)(X+Z)=X+YZ B. X(Y+Z)=XY+XZ C. X+XY=X
D. (X+Y)'=X'Y' (E.) X(X+Y)=X+Y

126. What statement is wrong?

A. (X+Y)(X+Z)=X+YZ B. X(Y+Z)=XY+XZ (C.) X+XY=X+Y
D. (X+Y)'=X'Y' E. X(X+Y)=X

127. What statement is wrong?

A. (X+Y)(X+Z)=X+YZ B. X(Y+Z)=XY+XZ C. X+XY=X
(D.) (X+Y)'=(XY)' E. X(X+Y)=X

128. What statement is wrong?

A. (X+Y)(X+Z)=X+YZ B. X(Y+Z)=XY+XZ C. X+XY=X
(D.) (XY)'=(X+Y)' E. X(X+Y)=X

129. A Boolean function is an expression, formed with

A. binary numbers
B. binary variables
C. binary variables and operators
(D.) binary variables, the two binary operators OR and AND, the unary operator NOT, parentheses, and equal sign.
E. binary variables, the binary operators OR, AND, and NOT, parentheses, and equal sign.

130. Exclusive-OR is called odd function, because

(A.) it is equal to 1 if the input variables have an odd number of 1's
B. it is equal to 1 if the input variables have an odd number of 0's
C. it is equal to 0 if the input variables have an odd number of 1's
D. it is equal to 0 if the input variables have an odd number of 0's
(E.) it is equal to 1 if the input variables have an odd number of 1's or 0's

131. The equivalence function is an even function, because

A. it is equal to 1 if the input variables have an even number of 0's or 1's
B. it is equal to 0 if the input variables have an even number of 1's
C. it is equal to 0 if the input variables have an even number of 0's
D. it is equal to 1 if the input variables have an even number of 1's
E. it is equal to 1 if the input variables have an even number of 0's

132. Which function is in nonstandard form?

A. (AB+CD)(A'B'+C'D) B. ABC+C'D C. ABC+CD
D. (A+B)(C+D) E. (A+C)(B+D)(A+D)

133. Which function is in canonical form?

A. (AB+CD)(A'B'+C'D) B. (ABC+C'D)(A+E) C. (ABC+CD)(AE+BC)
D. (A+BE)(BC+DE) E. (A+B+C+D')(A'+B+ C'+D)

134. The dual of F=XYZ'+X'YZ' is

A. (X'+Y'+Z)(X+Y'+Z) B. (XYZ')'+(X'YZ')' C. (X+Y+Z)(X+Y'+Z)
D. (X+Y+Z)'(X'+Y+Z')' E. (X+Y+Z')(X'+Y+Z')

135. The complement of F=XYZ'+X'YZ' is

A. (X'+Y'+Z)(X+Y'+Z) B. (XYZ')'+(X'YZ')' C. (X+Y+Z)(X+Y'+Z)
D. (X+Y+Z)'(X'+Y+Z')' E. (X+Y+Z')(X'+Y+Z')

136. According to the truth table function F_1 is equal to function _____

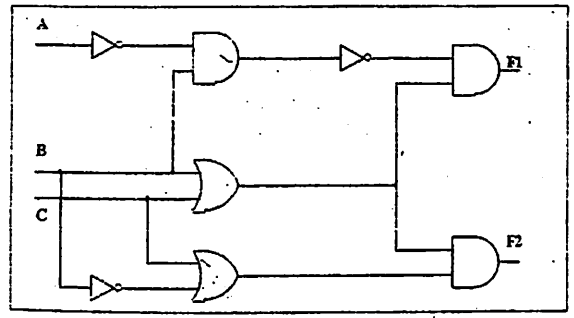
X	Y	Z	F_1	F_2	F_3	F_4	F_5	F_6
0	0	0	1	1	1	1	1	0
0	0	1	0	1	0	0	0	0
0	1	0	1	1	0	1	1	1
0	1	1	0	0	0	0	1	0
1	0	0	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0

A. $F_1 = F_2$ B. $F_1 = F_3$ C. $F_1 = F_4$ D. $F_1 = F_5$ E. $F_1 = F_6$

137. Simplification of the Boolean function F=BC+AC'+AB+BCD to a minimum number of literals gives us:

A. BC+AC B. B+AC C. BC+A D. BC+AB E. BC+AC'

138. The Boolean function F_1 for the following circuit is equal to:



A. (A+B')(B+C) B. (A+B)(B'+C) C. (A+C)(B'+C) D. C E. B+C

139. What fragment corresponds to definition of the Gray code?

A

x	y	F
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

B

x	y	F
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1

C

x	y	F
0	0	0
0	0	1
0	1	1
0	1	0
1	0	0

D

x	y	F
0	0	0
1	0	0
1	0	1
1	1	0
1	1	1

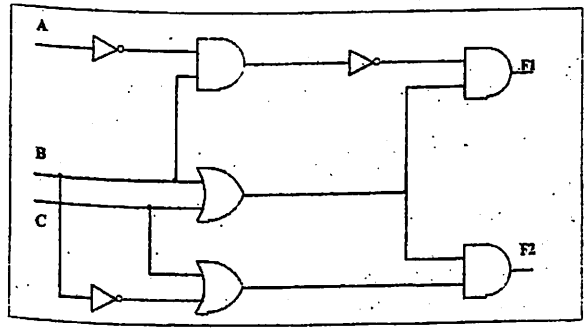
E

x	y	F
0	0	0
1	0	0
1	1	1
1	1	0
1	0	1

140. Binary addition of 10010011 and 01001011 gives us:
A. 10011110 B. 1011110 C. 11011010 D. 11010110 E. 11011110

141. Binary subtraction of 10011010-00110110 gives us:
A. 10011100 B. 1000100 C. 01100100 D. 10100100 E. 11000100

142. The Boolean function F_2 for the following circuit is equal to:



A. (A+B')(B+C) B. (A+B)(B'+C) C. (A+C)(B'+C) D. C E. B+C

143. Subtraction $(345)_8$-$(256)_8$ gives us:
A. 57 B. 66 C. 56 D. 156 E. 67

144. A feedback path is a connection from the output of one gate. to

A the output of a second gate
B the input of a second gate
C the input of a second gate that forms part of the input to the first gate
D. the input of a second gate that forms part of the input to the second gate
E. the output of a second gate that forms part of the input to the first gate

145. A code converter is a circuit that

A. makes the several systems compatible
B. makes the two systems compatible
C. makes the two systems compatible even though each uses a different binary code
D. makes the two systems compatible even though each uses a different codes
E. makes the several systems compatible even though each uses a different binary code

146. The 8's complement of $(754)_9$ is equal to

A. 121 B. 134 C. 123 D. 124 E. 234

147. The 15's complement of $(AB6)_{16}$ is equal to

A. 348 B. 349 C. 439 D. 538 E. 549

148. Decimal 3 will be represented in 8,4,-2,-1 code as

A. 0111 B. 0101 C. 0110 D. 0100 E. 1000

149. Decimal 8 will be represented in 2,4,2,1 code as

A. 0111 B. 0101 C. 0110 D. 1100 E. 1110

150. A combinational circuit consists of

A. input and output variables
B. logic gates
C. logic gates with feedback
D. input variables, logic gates, and output variables
E. input variables, logic gates with feedback, and output variables

151. A binary parallel adder is a digital function that produces:

A. the sum of two binary numbers
B. the arithmetic sum of two binary numbers
C. the sum of two binary numbers in parallel
D. the arithmetic sum of two binary numbers in parallel
E. the sum of two binary numbers and carry in parallel

152. What are don't care conditions for the function F=A′B′C′D+A′BC+AB′C if its simplification gives us F=A′C+B′C+A′B′?

A. d=A′B′+A′D B. d=A′C′+A′D C. d=A′B′C+A′B′D′
D. d=A′B′C+A′D E. d=A′B′C+A′BD′

153. What are don't care conditions for the function F=A′B+AB′C′ if its simplification gives us F=A′+B′C′?

A. d=A′B′C B. d=A′C′ C. d=A′B′C+A′B
D. d=A′B′C′ E. d=A′B′

154. What is a product of binary multiplication of 1101 and 10111?

A. 11001111 B. 10101111 C. 10001011 D. 10001101 E. 10001111

155. The sum of 4F and 2D in hex is equal to:

A. 8C B. 7D C. 7C D. 6D E. 6C

156. Subtraction D7-A8 in hex gives us:

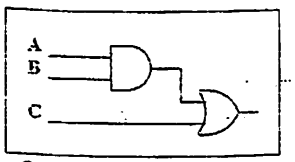
A. 3E B. 2D C. 3D D. 2F E. 3F

157. We have got map 1 and map 2. They are for functions _____ correspondently

		1		1	2	1		1	
	1		1				1		1

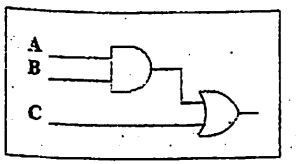
A. A⊕B⊕C and A⊕B⊙C B. A⊕B⊙C and A⊙B⊕C C. A⊙B⊕C and A⊕B⊙C
D. A⊕B⊕C and A⊙B⊙C E. A⊙B⊙C and A⊕B⊕C

158. The following circuit can be implemented with ____ NAND gates (all normal and complemented inputs are available).



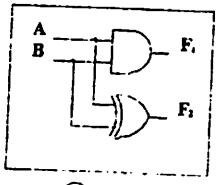
A. 1 B. 2 C. 3 D. 4 E. 5

159. The following circuit can be implemented with ____ NOR gates (all normal and complemented inputs are available).



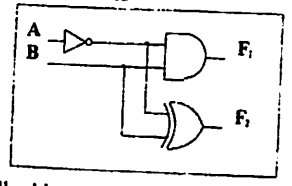
A. 1 B. 2 C. 3 D. 4 E. 5

160. This circuit is



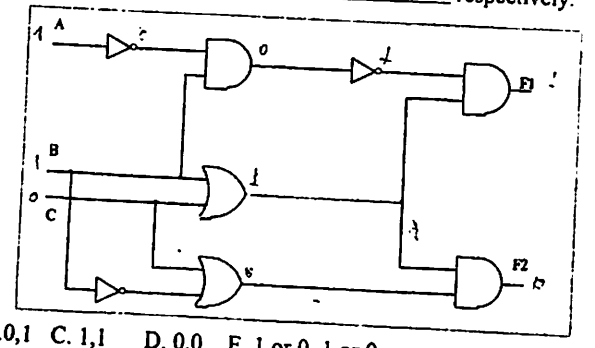
A. full-adder (B) Half-adder C. Full-subtractor D. Half-subtractor
E. none of the above mentioned

161. This circuit is



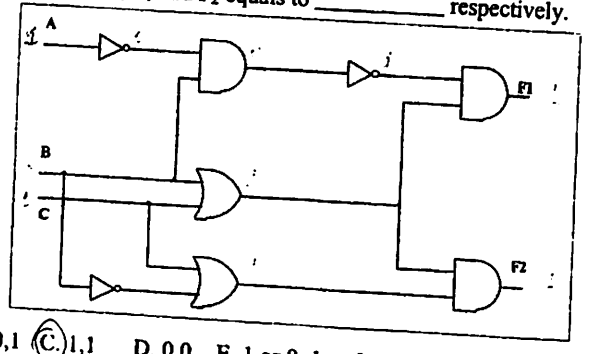
A. full-adder B. Half-adder C. Full-subtractor (D.) Half-subtractor
E. none of the above mentioned

162. If A=1, B=1,C=0, F_1 and F_2 equals to _____ respectively.



(A.) 1,0 B.0,1 C. 1,1 D. 0,0 E. 1 or 0, 1 or 0

163. If A=1, B=0,C=1, F_1 and F_2 equals to _____ respectively.



A. 1,0 B.0,1 (C.) 1,1 D. 0,0 E. 1 or 0, 1 or 0

164. A parity generator is a circuit, that
A. receives the parity bit
B. receives the parity bit from the transmitter
(C.) generates the parity bit in the transmitter
D. generates the parity bit
E. generates the parity bit for the transmitter

165. A parity checker is a circuit, that

A. receives the parity bit
B. receives the parity bit from the transmitter
C. check the parity bit
D. check the parity bit in the transmitter
(E.) check the parity in the receiver

166. A parity bit is an extra bit included with

(A.) a binary message to make the number of 1's either odd or even
B a binary message to make the number of 0's either odd or even
C a message to make the number of 1's either odd or even
D a binary message to make the number of 1's odd
E a binary message to make the number of 1's even

167. The operator _____ is called unary operator.

A. XOR B. AND C. OR D. XNOR (E.) NOT

168. The operator _____ is called binary operator.

A. XOR B. buffer (C.) OR D. XNOR E. NOT

169. The operator _____ is called binary operator.

A. XOR (B.) AND C. buffer D. XNOR E. NOT

170. Operation NOT can be represented by_____ NAND gate(s).

(A.) 1 B. 2 C. 1 or 2 D. 3 E. 2 or 3

171. Operation AND can be represented by_____ NAND gate(s).

A. 1 (B.) 2 C. 1 or 2 D. 3 E. 2 or 3

172. Operation OR can be represented by_____ NAND gate(s).

A. 1 B. 2 C. 1 or 2 (D.) 3 E. 2 or 3

173. Operation NOT can be represented by_____ NOR gate(s).

(A.) 1 B. 2 C. 1 or 2 D. 3 E. 2 or 3

174. Operation OR can be represented by_____ NOR gate(s).

A. 1 B. 2 C. 1 or 2 D. 3 E. 2 or 3

175. Operation AND can be represented by_____ NOR gate(s).

A. 1 B. 2 C. 1 or 2 D. 3 E. 2 or 3

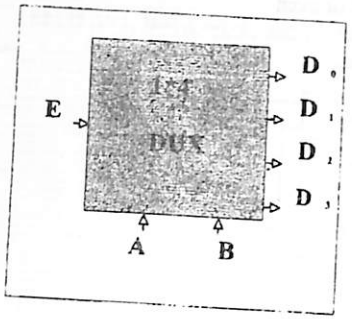
176. For priority encoder we have got input lines D_1, D_2, and D_5 active simultaneously such case output signal will be corresponded to …

A. D_1 B. D_2 C. D_5 D. D_1or D_2 E. D_2 or D_5

177. For priority encoder we have got input lines D_1, D_4, and D_6 active simultaneously such case output signal will be corresponded to …

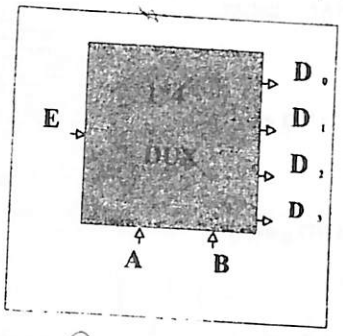
A. D_1 B. D_4 C. D_0 D. D_1or D_4 E. D_4 or D_6

178. What output of 1*4 demultiplexer will be chosen if selection linesAB=10?



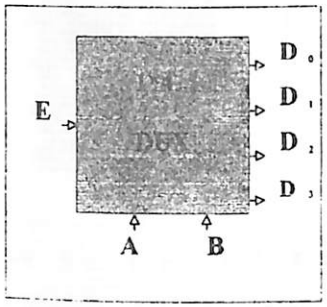
A. D_1 B. D_0 C. D_2 D. D_3 E. any of them

179. What output of 1*4 demultiplexer will be chosen if selection linesAB=00?



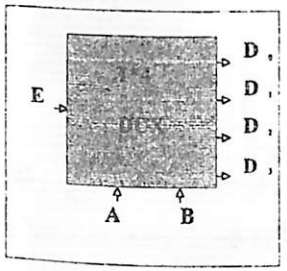
A. D_1 B. D_0 C. D_2 D. D_3 E. any of them

180. What output of 1*4 demultiplexer will be chosen if selection linesAB=01?



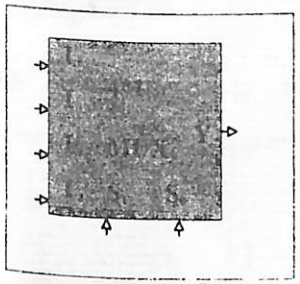
A. D_1 B. D_0 C. D_2 D. D_3 E. any of them

181. What output of 1*4 demultiplexer will be chosen if selection linesAB=11?



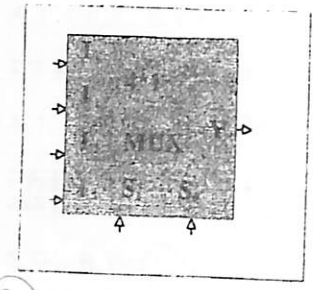
A. D_1 B. D_0 C. D_2 D. D_3 E. any of them

182. What will the output signal of 4*1 multiplexer be if selection lines S_1S_0=11?



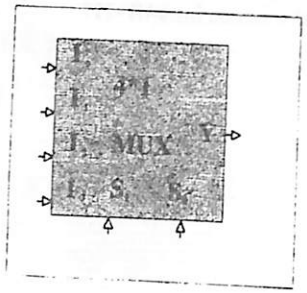
A. I_0 B. I_1 C. I_2 D. I_3 E. any of them

183. What will the output signal of 4*1 multiplexer be if selection lines S_1S_0=00?



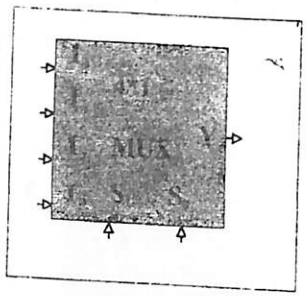
A. I_0 B. I_1 C. I_2 D. I_3 E. any of them

184. What will the output signal of 4*1 multiplexer be if selection lines S_1S_0=01?



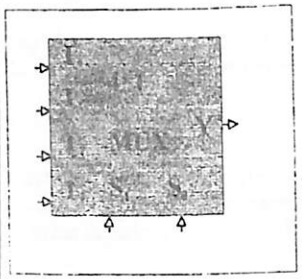
A. I_0 B. I_1 C. I_2 D. I_3 E. any of them

185. What will the output signal of 4*1 multiplexer be if selection lines S_1S_0=10?



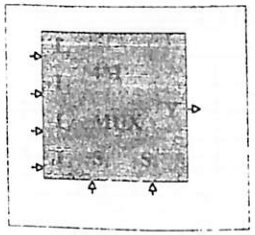
A. I_0 B. I_1 C. I_2 D. I_3 E. any of them

186. What are selection lines of 4*1 multiplexer if output signal $Y=I_0$?



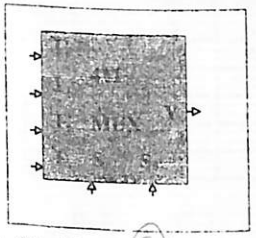
A. 00 B. 01 C. 10 D. 11 E. any of them

187. What are selection lines of 4*1 multiplexer if output signal $Y=I_1$?



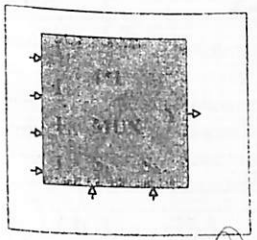
A. 00 B. 01 C. 10 D. 11 E. any of them

188. What are selection lines of 4*1 multiplexer if output signal $Y=I_2$?



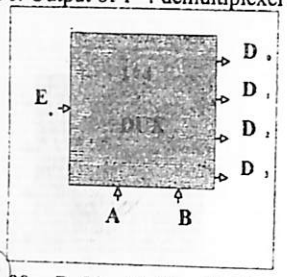
A. 00 B. 01 C. 10 D. 11 E. any of them

189. What are selection lines of 4*1 multiplexer if output signal $Y=I_3$?



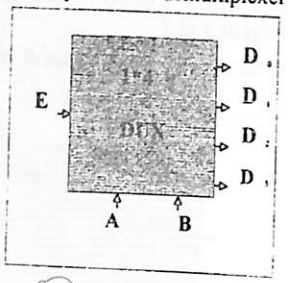
A. 00 B. 01 C. 10 D. 11 E. any of them

190. Output of 1*4 demultiplexer is D_0. What are selection lines?



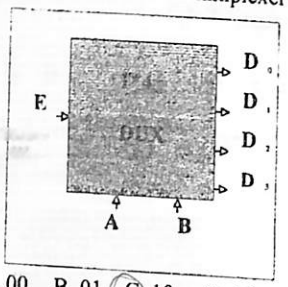
A. 00 B. 01 C. 10 D. 11 E. any of them

191. Output of 1*4 demultiplexer is D_1. What are selection lines?



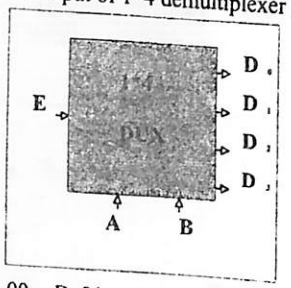
A. 00 B. 01 C. 10 D. 11 E. any of them

192. Output of 1*4 demultiplexer is D_2. What are selection lines?



A. 00 B. 01 C. 10 D. 11 E. any of them

193. Output of 1*4 demultiplexer is D_3. What are selection lines?



A. 00 B. 01 C. 10 D. 11 E. any of them

194. Where is a parity generator situated?

A. anywhere B. In the receiver C. In the transmitter
D. In the receiver and in the transmitter E. In the receiver or in the transmitter

195. Where is a parity checker situated?

A. anywhere B. In the receiver C. In the transmitter
D. In the receiver and in the transmitter E. In the receiver or in the transmitter

196. What decoder can work as demultiplexer?

A. 2*4 B. 3*8 C. 4*16 D. With enable E. any

197. For odd-parity checker the error is in the _____ row.

# of row	Four-bits received				Parity-error check
	x	y	Z	P	C
1	0	0	0	1	0
2	0	1	0	0	0
3	1	0	1	1	0
4	0	0	1	1	1
5	1	1	1	0	0

A.1 B. 2 C. 3 D.4 E.5

198. For even-parity checker the error is in the _____ row.

# of row	Four-bits received				Parity-error check
	x	y	Z	P	C
1	0	0	0	0	0
2	0	1	0	1	0
3	1	0	1	0	0
4	0	0	1	1	0
5	1	1	1	0	1

A.1 B. 2 C. 3 D.4 E.5

199. For odd-parity generator 1 for parity bit must be generated in the ___ row.

# of row	three-bit message		
	X	y	Z
1	0	0	1
2	0	1	0
3	1	0	1
4	1	0	0
5	1	1	1

A.1 B. 2 C. 3 D.4 E.5

200. For even-parity generator 1 for parity bit must be generated in the ___ row.

# of row	three-bit message		
	X	y	Z
1	0	0	0
2	0	1	1
3	1	0	1
4	1	0	0
5	1	1	0

A.1 B. 2 C. 3 (D) 4 E.5

201. Where is look-ahead carry generator used?

A. in parity checker B. In the transmitter C. In the receiver
D. in half-adder (E.) In parallel binary adder

202. Data selector is the second name of

A. DUX (B) MUX C. Decoder D. Encoder E. none of them

203. An algorithm is

A. a set of steps to obtain the result
B. a procedure to obtain the result
C. a procedure that specifies a set of steps
(D.) a procedure that specifies a finite set of steps which, if followed, give the solution the problem
E. a procedure that specifies a set of steps which, if followed, give the solution of problem

204. A multiplexer is called a data selector, since it selects

A. inputs and steers the binary information to the outputs
(B) one of many inputs and steers the binary information to the output line
C. one of many inputs and steers the binary information to the outputs
D. inputs and steers the binary information to the output line
E. one of many inputs and steers the binary information to many of the outputs

205. A combinational circuit with one output function is preferable to implement with _____, but the one of many output functions is preferable to implement with _____.

A. decoder, MUX B. Decoder, DUX (C) MUX, decoder
D. MUX, DUX E. binary parallel adder, decoder

206. To construct 6-bit parallel adder we must use cascade of such full-adders IC s as

A. two 2-bit and two 1-bit B. three 2-bit (C) one 4-bit and one 2-bit
D. six 1-bit E. none of above mentioned, because 6-bit parallel adder IC exists itself

207. To construct 7-bit parallel adder we must use cascade of such full-adders IC s as

A. two 2-bit and three 1-bit B. three 2-bit and one 1-bit
C.one 4-bit and one 3-bit (D.) One 4-bit, one 2-bit, and one 1-bit
E. none of above mentioned, because 7-bit parallel adder IC exists itself

208. Programmable logic array (PLA) may be
A. programmed by mask programming
B. field programmable
C. erasable programmable
D. electrically alterable
(E.) mask-programmable and field programmable

209. PLA (programmable logic array) can generate the function of _____ form.

A. AND-OR B. OR-AND C. AND-OR-invert
(D.) AND-OR-invert and AND-OR E. OR-AND-invert

210. MUX can realize _____ function(s).

(A.) 1 B. 2 C. 3 D. 4 E. any number of

211. The ROM is a circuit of _____ implementation in _____form.

A. 2-level,... sum of products
(B.) 2-level,... sum of minterms
C. 3-level,... sum of products
D. 3-level,... sum of minterms
E. 2 or 3-level,... sum of products

212. The PLA is a circuit of _____ implementation in _____form.

A. 2-level,... sum of products
B. 2-level,... sum of minterms
C. 3-level,... sum of products
D. 3-level,... sum of minterms
(E.) 2 or 3-level,... sum of products

213. What factor is, as a rule, more important for the circuit?

A. number of gates B. Types of gates (C.) Propagation delay
D. number of levels of implementation D. None of above mentioned

214. For BCD addition for correction we add

A. 1001 (B.) 0110 C. 1100 D. 0101 E none of them

215. For BCD adder for correction we use

A. special circuit B. Additional FA C. Additional 4-bit FA
(D.) additional 4-bit parallel FA E. none of above mentioned

216. PLA is _____ component.

A. SSI B. MSI C. LSI D. VLSI E. SSI or MSI

217. ROM is _____ component.

A. SSI B. MSI C. LSI D. VLSI E. SSI or MSI

218. MUX is _____ component.

A. SSI B. MSI C. LSI D. VLSI E. SSI or MSI

219. DUX is _____ component.

A. SSI B. MSI C. LSI D. VLSI E. SSI or MSI

220. Decoder is _____ component.

A. SSI B. MSI C. LSI D. VLSI E. SSI or MSI

221. Encoder is _____ component.

A. SSI B. MSI C. LSI D. VLSI E. SSI or MSI

222. This is characteristic table of _____ flip-flop.

		Q (t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	?

A. RS B. set-dominate RS C. D D. JK E. T

223. This is characteristic table of _____ flip-flop.

		Q (t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

A. RS B. Clocked RS C. D D. JK E. T

224. This is characteristic table of _____ flip-flop.

	Q (t+1)
0	0
1	1

A. RS B. Clocked RS C. D D. JK E. T

225. This is characteristic table of _____ flip-flop.

	Q (t+1)
0	Q(t)
1	Q'(t)

A. RS B. Clocked RS C. D D. JK E. T

226. This is excitation table of _____ flip-flop.

Q(t)	Q (t+1)		
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

A. RS B. set-dominate RS C. D D. JK E. T

227. This is excitation table of _____ flip-flop.

Q(t)	Q (t+1)		
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

A. RS B. Clocked RS C. D D. JK E. T

228. This is excitation table of _____ flip-flop.

Q(t)	Q (t+1)	
0	0	0
0	1	1
1	0	0
1	1	1

A. RS B. Clocked RS C. D D. JK E. T

229. This is excitation table of _____ flip-flop.

Q(t)	Q (t+1)	
0	0	0
0	1	1
1	0	1
1	1	0

A. RS B. Clocked RS C. D D. JK E. T

230. What state sequence for Q(t+1) is correct?

S	R	Q (t+1)
0	0	
0	1	
1	0	
1	1	

A. 1, 0, Q(t), ? B. 1, 0,?, Q(t) C. Q(t), 0,1, ? D. Q(t), 0,1, 1 E. Q(t), 0,1,

231. What state sequence for Q(t+1) is correct?

J	K	Q (t+1)
0	0	
0	1	
1	0	
1	1	

A. 1, 0, Q(t), ? B. 1, 0,?, Q(t) C. Q(t), 0,1,Q'(t) D. Q(t), 0,1, 1 E. Q(t), 0,1,

232. What state sequence for Q(t+1) is correct?

D	Q (t+1)
0	
1	

A. 1,0 B. 0,1 C. 1, ? D. 0, ? E. Q'(t) , 1

233. What state sequence for Q(t+1) is correct?

T	Q (t+1)
0	
1	

A. 1,0 B. 0,1 C. 1, ? D. 0, ? E. Q(t), Q'(t)

234. What state sequence for input S is correct?

Q(t)	Q (t+1)	S	R
0	0		X
0	1		0
1	0		1
1	1		0

A. 0,1,1,0 B. 0,1,1,X C. 1,0,0,X D. 0,1,0,1 E. 0,1,0,X

235. What state sequence for input R is correct?

Q(t)	Q (t+1)	S	R
0	0	0	
0	1	1	
1	0	0	
1	1	X	

A. 0,1,1,0 B. 0,1,1,X C. 1,0,0,X D. X,0,1,0 E. 0,1,0,X

236. What state sequence for input J is correct?

Q(t)	Q (t+1)	J	K
0	0		X
0	1		X
1	0		1
1	1		0

A. 0,1,1,X B. 0,1,X,X C. 1,0,0,X D. X,0,1,0 E. 0,1,0,X

237. What state sequence for input K is correct?

Q(t)	Q (t+1)	J	K
0	0	0	
0	1	1	
1	0	X	
1	1	X	

A. 0,1,1,0 B. 0,1,1,X C. 1,0,0,X D. X,X,1,0 E. 0,1,0,X

238. What state sequence for input D is correct?

Q(t)	Q (t+1)	D
0	0	
0	1	
1	0	
1	1	

A. 0,1,1,X B. 0,1,X,X C. 1,0,0,X D. X,0,1,0 E. 0,1,0,1

239. What state sequence for input T is correct?

Q(t)	Q (t+1)	T
0	0	
0	1	
1	0	
1	1	

A. 0,1,1,0 B. 0,1,X,X C. 1,0,0,X D. X,0,1,0 E. 0,1,0,1

240. Flip-flop(s) _____ may be set-dominate.

A. RS B. D and T C. D D. JK E. T

241. Set-dominate flip-flop has got _____ input(s).

A. 1 B. 2 C. 1 or 2 D. 3 E. 2 or 3

242. A set-dominate flip-flop differs from a conventional_____ one in that an attempt _____ results in _____ the flip-flop.

A. JK, simultaneously set and reset, setting
B. JK, set and reset, setting
C. RS, simultaneously set and reset, setting
D. RS, set and reset, setting
E. RS, simultaneously set and reset, resetting

243. SR flip-flop characteristic equation is _____

A. Q(t+1)=SR B. Q(t+1)=S+R C. Q(t+1)=S+RQ
D. Q(t+1)=S+R′Q E. Q(t+1)=S+R′Q SR=0

244. D flip-flop characteristic equation is _____

A. Q(t+1)=DQ B. Q(t+1)=D+Q C. Q(t+1)=D
D. Q(t+1)=D′Q E. Q(t+1)=D′

245. JK flip-flop characteristic equation is _____

A. Q(t+1)=JK B. Q(t+1)=J+K C. Q(t+1)=J+KQ
D. Q(t+1)=J+K′Q E. Q(t+1)=JQ′+K′Q

246. T flip-flop characteristic equation is _____

A. Q(t+1)=TQ B. Q(t+1)=T+Q C. Q(t+1)= T′
D. Q(t+1)=T Q′+T′Q E. Q(t+1)=TQ+T′Q′

247. Next state of flip-flop is a function of

A. present state
B. Present state and the inputs
C. the inputs and the type of flip-flop used
D. Present state and the type of flip-flop used
E. the inputs, the present state and the type of flip-flop used

248. The state diagram of the sequential circuit

A. consists of circles and lines
B. is another view of the state table
C. is graphical representation of the state table
D. contains additional information about sequential circuit
E. shows only present state of the sequential circuit

249. A state equation of the sequential circuit is

A. an expression to describe next state of the circuit
B. an expression to describe present state of the circuit
C. a Boolean function that specifies the present state conditions
D. a Boolean function that specifies the present state conditions that make the next state equal to 1
E. a Boolean function that specifies the next state conditions that make the present state equal to 1

250. _____ fully specify a sequential circuit.

A. The state equations of all flip flops
B. The state equations of all flip flops and state diagram
C. The state equations of all flip flops, together with the output function
D. The state equations of all flip flops and state table
E. The type of flip-flops

251. For look-ahead carry generator the general expression for carry is

A. $C_{i+1}=G_i+P_iC_i$ B. $C_{i+1}=P_i+G_iC_i$ C. $C_{i+1}=G_i+C_i$
D. $C_{i+1}=G_i+P_i$ E. $C_{i+1}=G_{i+1}+P_iC_i$

252. Equation for carry output of the second stage of look-ahead carry generator is

A. $C_2=G_1+P_1C_1$ B. $C_2=G_1+P_1$ C. $C_2=G_1+C_1$ D. $C_2=G_1+P_2C_1$ E. $C_2=G_1+P_1C_2$

253. Equation for carry output of the third stage of look-ahead carry generator is

A. $C_3=G_2+P_1C_2$ B. $C_3=G_2+P_2C_2$ C. $C_3=G_1+P_1C_1$ D. $C_3=G_1+P_2C_1$ E. $C_3=G_2+P_1C_1$

254. Look-ahead carry generator is a circuit of _____ level implementation.
A.1 B.2 C. 1 or 2 D. 3 E. 2 or 3

255. Enable input is the input

A. to make a device active
B. to provide the normal device's operation
C. to control the circuit operation
D. to make the circuit sensitive
E. to have part of the circuit active

256. Flip-flop's setup time is a definite time, in which flip-flop's inputs must be maintained at

A. a constant value
B. a constant value prior to the application of pulse
C. a constant value prior to the application of clock pulse
D. a constant value after the application of pulse
E. a constant value after the application of clock pulse

257. Flip-flop's hold time is a definite time, in which

A. the input must not change after the application of the positive-going transition of clock pulse
B. the input must not change after the application of clock pulse
C. the input must change after the application of clock pulse
D. the input must change after the application of the positive-going transition of clock pulse
E. none of above mentioned answers

258. Function # _____ corresponds to function AND of 3 variables.

X	Y	Z	F_1	F_2	F_3	F_4	F_5
0	0	0	0	0	0	0	0
0	0	1	0	0	1	1	0
0	1	0	0	0	1	1	0
0	1	1	1	1	1	1	0
1	0	0	0	1	1	1	0
1	0	1	1	1	1	0	0
1	1	0	1	1	1	0	0
1	1	1	1	1	1	1	1

A. 1 B. 2 C. 3 D. 4 (E.) 5

259. Function # _____ corresponds to function NAND of 3 variables.

X	Y	Z	F_1	F_2	F_3	F_4	F_5
0	0	0	0	0	1	0	0
0	0	1	0	0	1	1	0
0	1	0	0	0	1	1	0
0	1	1	1	1	1	1	0
1	0	0	0	1	1	1	0
1	0	1	1	1	1	1	0
1	1	0	1	1	1	0	0
1	1	1	1	1	1	0	0

A. 1 B. 2 (C.) 3 D. 4 E. 5

260. Function # _____ corresponds to function OR of 3 variables.

X	Y	Z	F_1	F_2	F_3	F_4	F_5
0	0	0	0	0	0	0	0
0	0	1	0	0	1	1	0
0	1	0	0	0	1	1	0
0	1	1	1	1	1	1	0
1	0	0	0	1	1	1	0
1	0	1	1	1	1	0	0
1	1	0	1	1	1	0	0
1	1	1	1	1	1	1	1

A. 1 B. 2 (C.) 3 D. 4 E. 5

261. Function # _____ corresponds to function NOR of 3 variables.

X	Y	Z	F_1	F_2	F_3	F_4	F_5
0	0	0	0	0	0	0	1
0	0	1	0	0	1	1	0
0	1	0	0	0	1	1	0
0	1	1	1	1	1	1	0
1	0	0	0	1	1	1	0
1	0	1	1	1	1	0	0
1	1	0	1	1	1	0	0
1	1	1	1	1	1	1	0

A. 1 B. 2 C. 3 D. 4 (E.) 5

262. Function # _____ corresponds to function XNOR of 3 variables.

X	Y	Z	F_1	F_2	F_3	F_4	F_5
0	0	0	0	1	0	0	0
0	0	1	0	0	1	1	0
0	1	0	0	0	1	1	0
0	1	1	1	1	1	1	0
1	0	0	0	0	1	1	0
1	0	1	1	1	1	0	0
1	1	0	1	1	1	0	0
1	1	1	1	0	1	1	1

A. 1 (B.) 2 C. 3 D. 4 E. 5

263. Function # _____ corresponds to function XOR of 3 variables.

X	Y	Z	F_1	F_2	F_3	F_4	F_5
0	0	0	0	0	0	0	0
0	0	1	0	0	1	1	0
0	1	0	0	0	1	1	0
0	1	1	1	1	0	1	0
1	0	0	0	1	1	1	0
1	0	1	1	1	0	0	0
1	1	0	1	1	0	0	0
1	1	1	1	1	1	1	1

A. 1 B. 2 C. 3 D. 4 E. 5

264. What is the state equation for A(t+1) for the state table below?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	0
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	1

A. A(t+1)=ABX B. A(t+1)=ABX+ABX' C. A(t+1)=ABX+A'(B+X')
D. A(t+1)=ABX+A'(BX'+B'X) E. A(t+1)=ABX+A(BX'+B'X)

265. What is the state equation for B(t+1) for the state table below?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	0
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	1

A. B(t+1)=ABX B. B(t+1)=ABX+ABX' C. B(t+1)=ABX+A'(B+X')
D. B(t+1)=A'B'X' E. B(t+1)=A'B'X'+AB

266. What is the state equation for A(t+1) for the state table below?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	1	1	1	0
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	0	1

A. A(t+1)=ABX B. A(t+1)=ABX+ABX' C. A(t+1)=ABX+A'(B+X')
D. A(t+1)=ABX+A'(BX'+B'X) E. A(t+1)=A'(B'+X')

267. What is the state equation for B(t+1) for the state table below?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	0

A. B(t+1)=ABX B. B(t+1)=ABX'+A'B' C. B(t+1)=ABX+A'(B+X')
D. B(t+1)=ABX+A'(BX'+B'X) E. B(t+1)=ABX+A(BX'+B'X)

268. State equation for A flip-flop is A(t+1)=ABX+A'X'. Define correct state table for A.

Present state		Next state of A									
		1		2		3		4		5	
A	B	X=0	X=1	X=0	X=1	X=0	X=1	X=0	X=1	X=0	X=1
0	0	1	0	1	0	0	0	1	0	1	1
0	1	1	0	1	0	1	0	0	0	1	0
1	0	0	0	1	0	1	0	0	0	0	0
1	1	0	1	0	1	0	1	0	1	0	1

A. column 1 B. Column 2 C. Column3 D. Column 4 E. column 5

269. State equation for B flip-flop is B(t+1)=ABX+A'B'X'. Define correct state table for B.

Present state		Next state of B									
		1		2		3		4		5	
A	B	X=0	X=1	X=0	X=1	X=0	X=1	X=0	X=1	X=0	X=1
0	0	1	0	1	0	0	0	1	0	1	1
0	1	1	0	1	0	1	0	0	0	1	0
1	0	0	0	1	0	1	0	0	0	0	0
1	1	0	1	0	1	0	1	0	1	0	1

A. column 1 B. Column 2 C. Column3 D. Column 4 E. column 5

270. State equation for A flip-flop is A(t+1)=AB+A'B'. Define correct state table for A.

Present state		Next state of A									
		1		2		3		4		5	
A	B	X=0	X=1	X=0	X=1	X=0	X=1	X=0	X=1	X=0	X=1
0	0	1	0	1	0	0	0	1	0	1	1
0	1	1	0	1	0	1	0	0	0	0	0
1	0	0	0	1	0	1	0	0	0	0	0
1	1	0	1	0	1	0	1	0	1	1	1

A. column 1 B. Column 2 C. Column3 D. Column 4 E. column 5

271. Direct preset input of flip-flop is used

A. to set the flip-flop to an initial state B. to set the flip-flop
C. to set the flip-flop asynchronously
D. to set the flip-flop asynchronously during clock pulse occurrence
E to set the flip-flop asynchronously on a positive (or negative) value of the input sign

272. Direct clear input of flip-flop is used

A. to clear the flip-flop to an initial state B. to clear the flip-flop
C. to clear the flip-flop asynchronously
D. to clear the flip-flop asynchronously during clock pulse occurrence
E. to clear the flip-flop asynchronously on a positive (or negative) value of the input sig

273. Clocked sequential circuits are

A. asynchronous sequential circuits that use clock pulses in the inputs of memory elements
B. synchronous sequential circuits that use clock pulses in the inputs of memory elemen
C. sequential circuits that use clock pulses in the inputs of memory elements
D. asynchronous sequential circuits that use clock pulses
E. synchronous sequential circuits that use clock pulses

274. A sequential circuit is specified by

A. inputs and outputs B. Inputs, outputs, and internal states
C. Inputs and internal states
D. a time sequence of inputs, outputs, and internal states
E. a time sequence of inputs and internal states

275. D flip-flop is a _____ flip-flop with an inverter in the _____ input.

A. JK, .. set B. JK, ... reset C. RS, ...set
D. RS, ...reset E. clocked RS, ... reset

276. This is characteristic table of _____ flip-flop.

		Q (t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	1

A. RS (B.) Set-dominate RS C. D D. JK E. T

277. This is characteristic table of _____ flip-flop.

		Q (t+1)
0	0	0
0	1	Q(t)
1	0	Q'(t)
1	1	1

A. RS (B.) JK' C. D D. JK E. T

278. This is excitation table of _____ flip-flop.

Q(t)	Q (t+1)		
0	0	0	X
0	1	1	X
1	0	0	1
1	1	Case 1 X Case 2 1	Case 1 0 Case 2 X

A. RS (B.) Set-dominate RS C. D D. JK E. T

279. This is excitation table of _____ flip-flop.

Q(t)	Q (t+1)		
0	0	0	X
0	1	1	X
1	0	X	0
1	1	X	1

A. RS (B.) JK' C. D D. JK E. T

280. What state sequence for Q(t+1) is correct?

SD	R	Q (t+1)
0	0	
0	1	
1	0	
1	1	

A. 1, 0, Q(t), ? B. 1, 0,?, Q(t) C. Q(t), 0,1, ? D. Q(t), 0,1, 1 E. Q(t), 0,1, 0

281. What state sequence for Q(t+1) is correct?

J	K'	Q (t+1)
0	0	
0	1	
1	0	
1	1	

A. 1, 0, Q(t), ? B. 1, 0,?, Q(t) C. 0, Q(t),Q'(t), 1 D. Q(t), 0,1, 1 E. Q(t), 0,1, 0

282. What state sequence for input SD is correct?

Q(t)	Q (t+1)	SD	R
0	0		X
0	1		X
1	0		1
1	1		Case1 0 Case 2 X

A. 0,1,1,0 or 1 B. 0,1,1,X or 1 C. 1,0,0,X or 0 D. 0,1,0,1 or 0 E. 0,1,0,X or1

283. What state sequence for input R is correct?

Q(t)	Q (t+1)	SD	R
0	0	0	
0	1	1	
1	0	0	
1	1	Case1 X Case 2 1	

A. 0,1,1,0 or 1 B. 0,1,1,X or 1 C. 1,0,0,X or 1 D. X,X,1,0 or X E. 0,1,0,X or

284. What state sequence for input J is correct?

Q(t)	Q (t+1)	J	K'
0	0		X
0	1		X
1	0		0
1	1		1

A. 0,1,1,X B. 0,1,X,X C. 1,0,0,X D. X,0,1,0 E. 0,1,0,X

285. What state sequence for input K' is correct?

Q(t)	Q (t+1)	J	K'
0	0	0	
0	1	1	
1	0	X	
1	1	X	

A. 0,1,1,0 B. 0,1,1,X C. 1,0,0,X D. X,X,0,1 E. 0,1,0,X

286. SR set-dominate flip-flop characteristic equation is _____

A. Q(t+1)=SR B. Q(t+1)=S+R C. Q(t+1)=S+RQ D. Q(t+1)=S+R´Q
E. Q(t+1)=S+R´Q SR=0

287. How many options to gain state 00 will the circuit with the state table below have?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	0

A. 1 B. 2 C. 3 D. 4 E. 5

288. How many options to gain state 01 will the circuit with the state table below have?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	0

A. 1 B. 2 C. 3 D. 4 E. 5

289. How many options to gain state 10 will the circuit with the state table below have?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	0

A. 1 B. 2 C. 3 D. 4 E. 5

290. How many options to gain state 11 will the circuit with the state table below have?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	0

A. 1 B. 2 C. 3 D. 4 E. 5

291. Resistor has got 4 strips on its case. They are situated from the left to the right in such order: yellow, blue, red, golden. What is the nominal value of resistance?

A. 220 Ù B. 1kÙ C. 330 Ù D. 4.6 kÙ E. 10 kÙ

292. Resistor has got 4 strips on its case. They are situated from the left to the right in such order: red, red, brown, golden. What is the nominal value of resistance?

A. 220 Ù B. 1kÙ C. 330 Ù D. 4.6 kÙ E. 10 kÙ

293. Resistor has got 4 strips on its case. They are situated from the left to the right in such order: brown, black, orange, golden. What is the nominal value of resistance?

A. 220 Ù B. 1kÙ C. 330 Ù D. 4.6 kÙ E. 10 kÙ

294. Resistor has got 4 strips on its case. They are situated from the left to the right in s order: brown, black, red, golden. What is the nominal value of resistance?

A. 220 Ù (B) 1kÙ C. 330 Ù D. 4.6 kÙ E. 10 kÙ

295. Resistor has got 4 strips on its case. They are situated from the left to the right in s order: orange, orange, brown, golden. What is the nominal value of resistance?

A. 220 Ù B. 1kÙ (C) 330 Ù D. 4.6 kÙ E. 10 kÙ

296. Value of resistance is 100 Ù. It means that the first three strips on the resistance cas (in whole the case has got 4 strips) are:

A. red, brown, red B. Red, brown, black C. Black, brown, red
(D.) brown, black, brown E. brown, black, red

297. Value of resistance is 47 kÙ. It means that the first three strips on the resistance cas (in whole the case has got 4 strips) are:

A. red, green, red B. Red, brown, black (C.) Yellow, violet, orange
D. yellow, black, brown E. brown, black, orange

298. Value of resistance is 560 Ù. It means that the first three strips on the resistance cas (in whole the case has got 4 strips) are:

A. red, brown, blue (B.) Green, blue, brown C. Black, brown, red
D. brown, black, white E. violet, black, red

299. Value of resistance is 100 kÙ. It means that the first three strips on the resistance cas (in whole the case has got 4 strips) are:

A. red, brown, red B. Red, brown, black C. Black, brown, blue
(D.) brown, black, yellow E. brown, black, orange

300. Value of resistance is 9.6 kÙ. It means that the first three strips on the resistance cas (in whole the case has got 4 strips) are:

(A.) white, blue, red B. gray, brown, black C. Black, brown, green
D. brown, black, brown E. brown, black, red

301. The first strip to obtain resistance 100 Ù must be

A. white B. Green (C.) Brown D. Yellow E. red

302. The first strip to obtain resistance 220 Ù must be

A. white B. Green C. Brown D. Yellow (E.) red

303. The first strip to obtain resistance 330 Ù must be

(A.) orange B. Green C. Brown D. Yellow E. red

304. The first strip to obtain resistance 460 Ù must be

A. white B. Green C. Brown (D.) Yellow E. red

305. The first strip to obtain resistance 5 kÙ must be

A. white (B.) Green C. Brown D. Yellow E. red

306. The first strip to obtain resistance 6 kÙ must be

A. white B. Green C. Brown D. Yellow (E.) blue

307. The first strip to obtain resistance 780 Ù must be

A. white B. Green (C.) violet D. Yellow E. red

308. The first strip to obtain resistance 80 Ù must be

A. white B. Green C. Brown D. Yellow (E.) gray

309. The first strip to obtain resistance 90 Ù must be

(A.) white B. Green C. Brown D. Yellow E. red

310. The second strip to obtain resistance 120 Ù must be

A. white B. Green C. Brown D. Yellow (E.) red

311. The second strip to obtain resistance 180 Ù must be

A. white B. Green C. Brown D. Yellow (E.) gray

312. The second strip to obtain resistance 1.2 kÙ must be

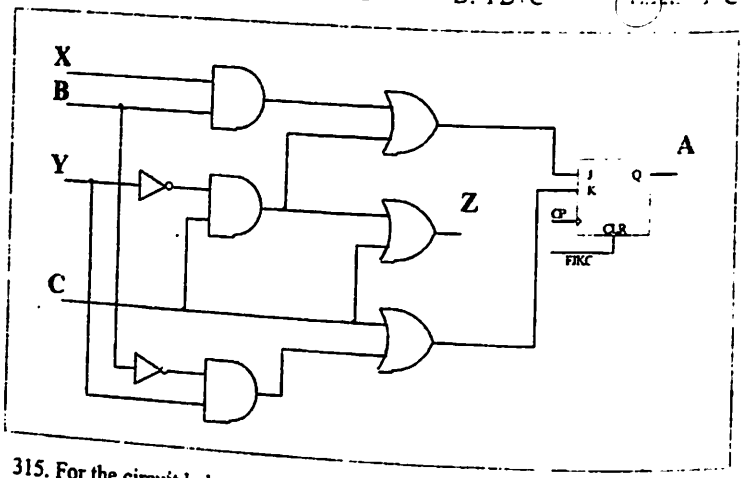
A. white B. Green C. Brown D. Yellow (E.) red

313. The second strip to obtain resistance 560 Ù must be

(A.) blue B. Green C. Brown D. Yellow E. red

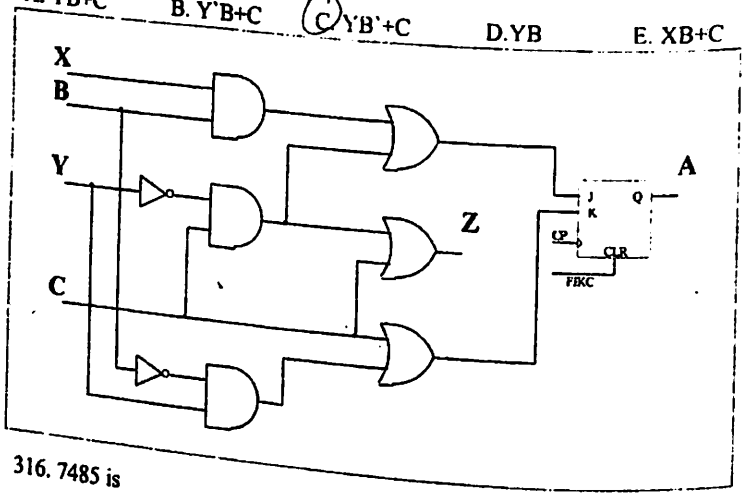
314. For the circuit below input equation for J is

A. XB+YC B. XB C. YC D. YB+C E. XB+Y`C



315. For the circuit below input equation for K is

A. YB+C B. Y`B+C  C. Y`B`+C D.YB E. XB+C



316. 7485 is

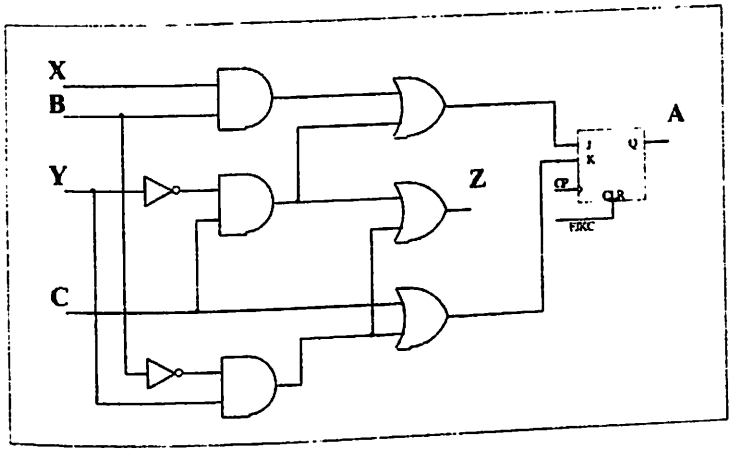
A. 3*8 decoder B. 4-bit magnitude comparator C. Code converter
D. D flip-flop E. priority encoder

317. 74138 is

A. 1*8 decoder/ demultiplexer B. 4-bit magnitude comparator
C. Code converter D. D flip-flop E. priority encoder

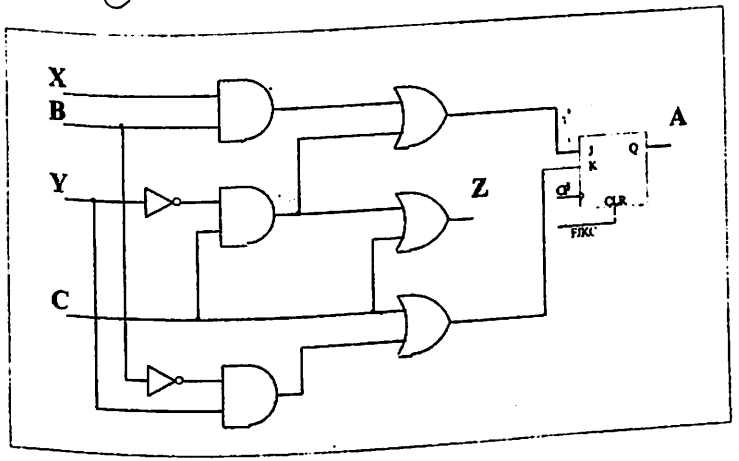
318. For the circuit below output Z is equal to

A. Y`C+YB  B. Y`C+B`Y  C. YC+Y`B D. Y`C+B` E. YB+B`C



319. For the circuit below if X=0, B=0, Y=1, C=1 the next state is __(active signal 1)

A. set B. reset C. No change D. complement E. set or no change



320. 7447 is

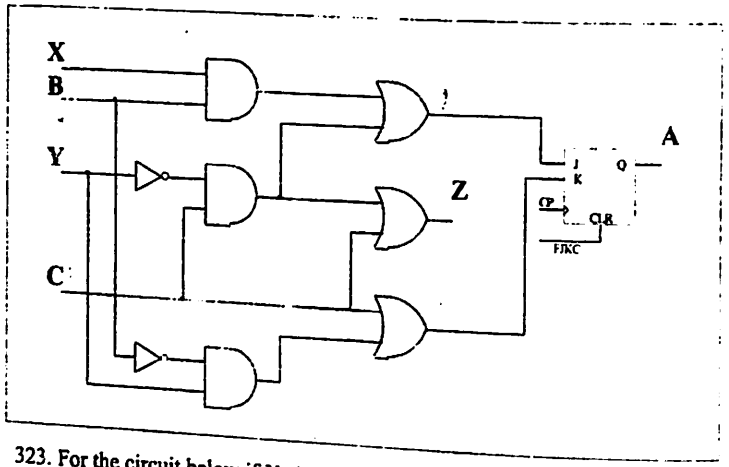
A. 3*8 decoder B. 4-bit magnitude comparator C. priority encoder
D. D flip-flop E. BCD-to-seven-segment decoder/driver

321. 7474 is

A. 3*8 decoder B. 4-bit magnitude comparator C. priority encoder
D. D flip-flop E. BCD-to-seven-segment decoder/driver

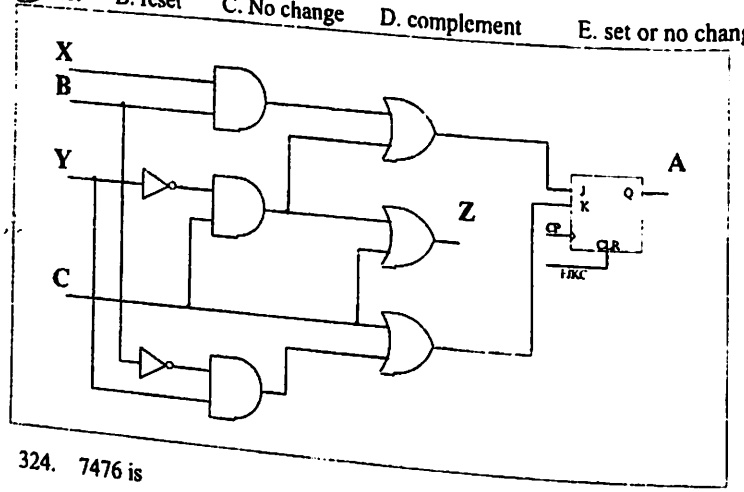
322. For the circuit below if X=0, B=0, Y=0, C=1 the next state is __(active signal 1)

A. set B. reset C. No change D. complement E. set or no change



323. For the circuit below if X=1, B=1, Y=0, C=0 the next state is __(active signal 1)

A. set B. reset C. No change D. complement E. set or no change



324. 7476 is

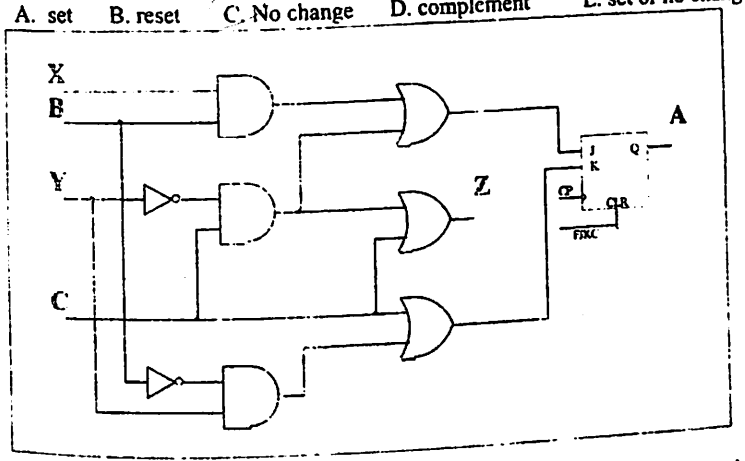
A. 3*8 decoder B. 4-bit magnitude comparator C. priority encoder
D. JK flip-flop E. BCD-to-seven-segment decoder/driver

325. 74148 is

A. 3*8 decoder B. 4-bit magnitude comparator C. priority encoder
D. D flip-flop E. BCD-to-seven-segment decoder/driver

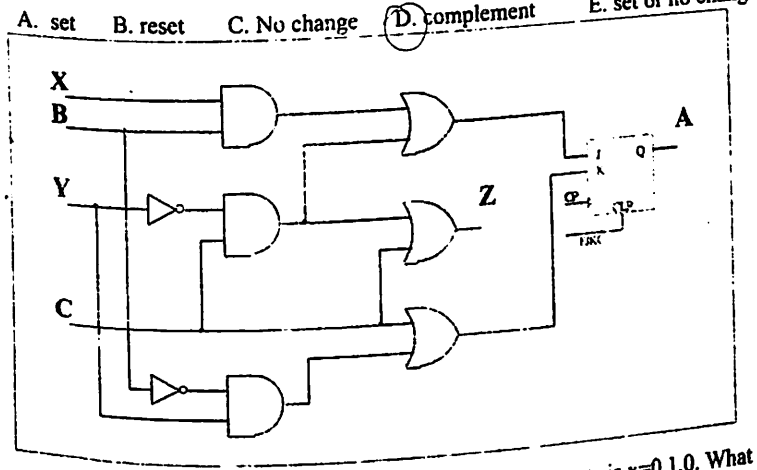
326. For the circuit below if X=0, B=0, Y=0, C=0 the next state is __(active signal 1)

A. set B. reset C. No change D. complement E. set or no change



327. For the circuit below if X=1, B=1, Y=0, C=1 the next state is __(active signal 1)

A. set B. reset C. No change D. complement E. set or no change



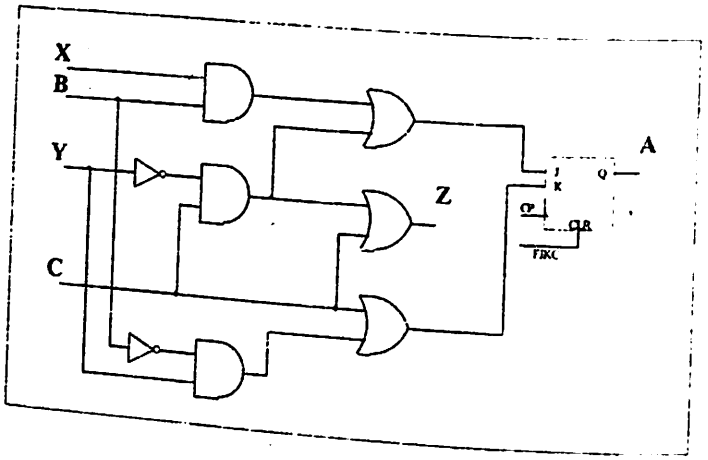
328. Present state of the flip-flops AB=01. Sequence of inputs is x=0,1,0. What will be the sequence of next states of the circuit with the state table below?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	0

A. 01,00,01 B. 10,00,01 C. 10,10,01 D. 10,00,00 E. 00,01,01

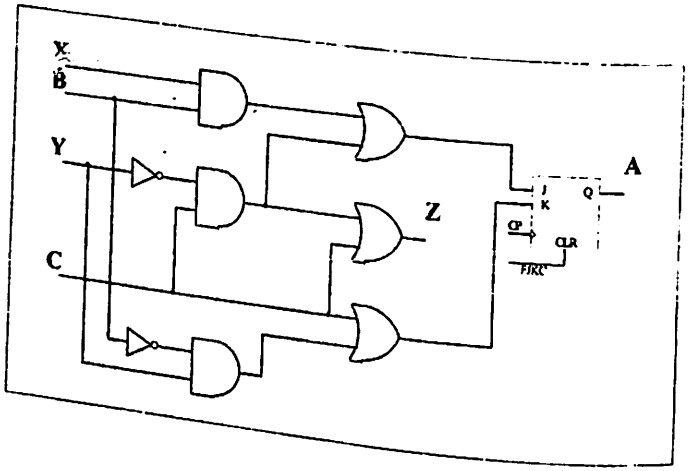
329. For the circuit below X=1,B=1. What value must have Y and C to obtain complement state for the flip-flop? (x-don't-care conditions)

A. x, 0 B.x,1 C.1,x D. 0,x E. none



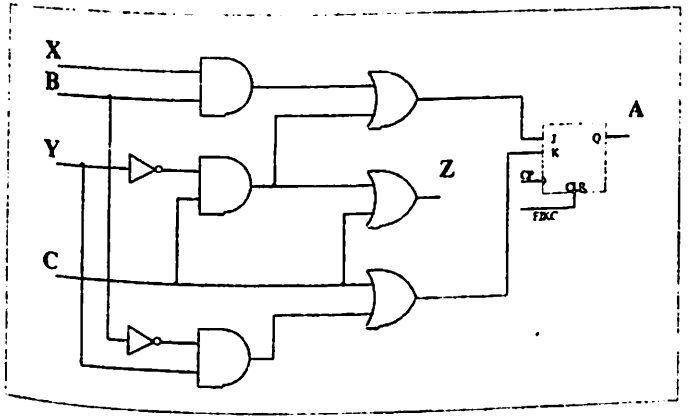
330. For the circuit below X=1,B=1. What value must have Y and C to obtain "no change" state for the flip-flop? (x-don't-care conditions)

A. x, 0 B.x,1 C.1,x D. 0,x E. none



331. For the circuit below X=0,B=0. What value must have Y and C to obtain complement state for the flip-flop? (x-don't-care conditions)

A. x, 0 B.0,1 C.1,x D. 0,0 E. none



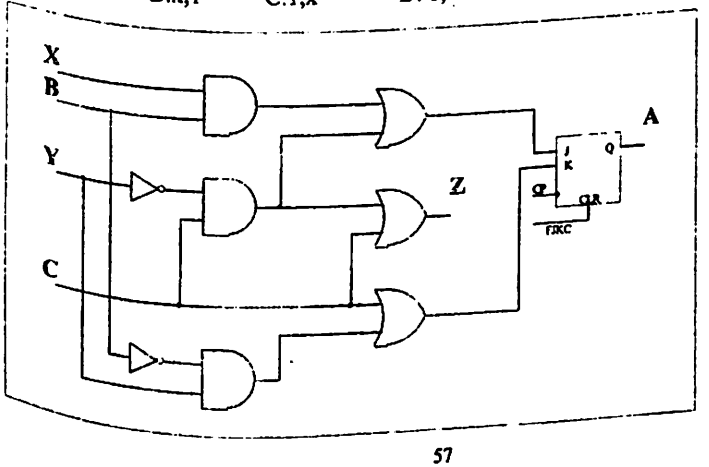
332. Present state of the flip-flops AB=10. Sequence of inputs is x=0,1,0. What will be the sequence of next states of the circuit with the state table below?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	0

A. 01,00,01 B. 10,00,01 C. 10,10,01 D. 10,00,00 E. 00,11,01

333. For the circuit below X=1,B=0. What value must have Y and C to obtain "no change" state for the flip-flop? (x-don't-care conditions)

A. 0, 0 B.x,1 C.1,x D. 0,1 E. none



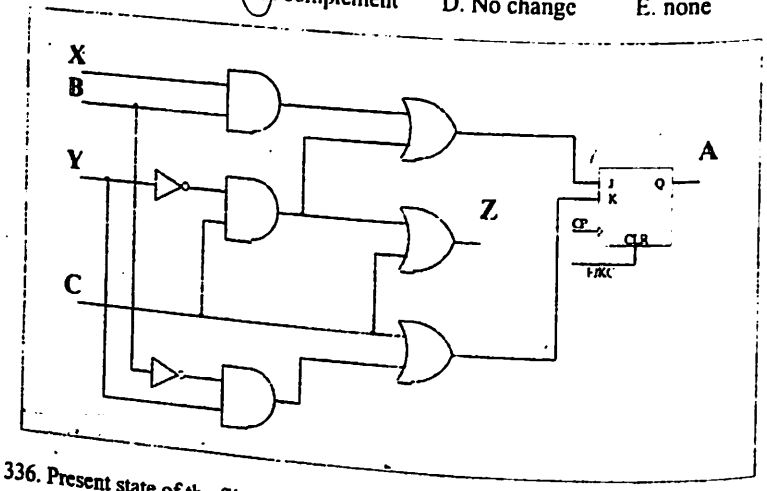
334. Present state of the flip-flops AB=00. Sequence of inputs is x=0,0,1. What will be the sequence of next states of the circuit with the state table below?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	0

A. 01,10,00 B. 10,00,01 C. 10,10,01 D. 10,00,00 E. 00,01,01

335. For the circuit below X=1,B=1,Y=1,C=1. What will be the next state for the flip-flop?

A. set B. reset C. complement D. No change E. none



336. Present state of the flip-flops AB=00. Sequence of inputs is x=1,1,0. What will be the sequence of next states of the circuit with the state table below?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	0

A. 01,00,01 B. 10,00,01 C. 11,10,00 D. 10,00,00 E. 00,01,01

337. Present state of the flip-flops AB=11. Sequence of inputs is x=0,1,0. What will be the sequence of next states of the circuit with the state table below?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	0

A. 01,00,01 B. 10,00,01 C. 10,10,01 D. 10,00,00 E. 00,01,01

338. Present state of the flip-flops AB=11. Sequence of inputs is x=1,1,0. What will be the sequence of next states of the circuit with the state table below?

Present state		Next state			
		X=0		X=1	
A	B	A	B	A	B
0	0	0	1	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	1	0	1	1	0

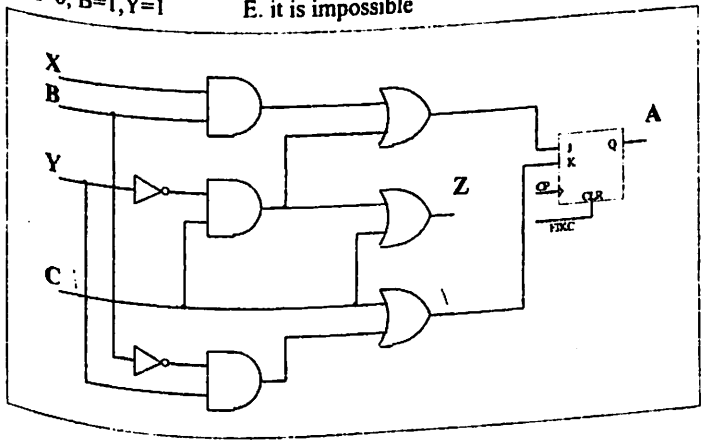
A. 01,00,01 B. 10,00,01 C. 10,10,01 D. 10,00,00 E. 00,01,01

339. It needs to convert JK flip-flop into D flip-flop. For this purpose we must

A. connect J and K inputs together B. Use inverter for J input
C. use inverter for K input
D. use inverter for J input and connect inverter's input with K input
E. use inverter for K input and connect inverter's input with J input

340. For the circuit below if C= 1 and present state of A is set to obtain reset state it needs to have (x-don't –care conditions)

A. X=x,B=x,Y=x B.X=1, B=0,Y=1 C. X=0, B=0,Y=1
D. X=0, B=1,Y=1 E. it is impossible



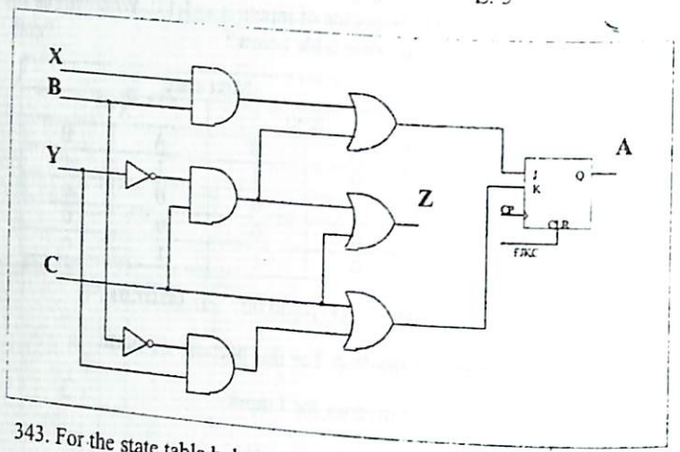
341. For the state table below define the values of T_{A1} column.

A1	A0	T_{A1}	T_{A0}
0	0		1
0	1		1
1	0		1
1	1		1

A. 1,0,1,0 B. 0,1,0,1 C. 1,0,0,1 D. 0,1,1,0 E. 1,1,0,0

342. How many levels of implementation the combination part of the circuit below has?

A. 1 B. 2 C. 3 D. 4 E. 5



343. For the state table below define the values of T_{A0} column.

A1	A0	T_{A1}	T_{A0}
0	0	0	
0	1	1	
1	0	0	
1	1	1	

A. 1,0,1,0 B. 0,1,0,1 C. 1,0,0,1 D. 0,1,1,0 E. 1,1,1,1

344. For the state table below define the T_{A1} input function. T_{A1}= _____

A1	A0	T_{A1}	T_{A0}
0	0	0	1
0	1	1	1
1	0	0	1
1	1	1	1

A. A_0 B. 1 C. 0 D. A_1 E. $A`_1$

345. For the state table below define T_{A0} input function. T_{A0}= _____

A1	A0	T_{A1}	T_{A0}
0	0	0	1
0	1	1	1
1	0	0	1
1	1	1	1

A. A_0 B. 1 C. 0 D. A_1 E. $A`_1$

346. For the state table below define the values of T_{A0} column.

A1	A0	T_{A1}	T_{A0}
0	0	0	
0	1	1	
1	0	1	

A. 1,0,1 B. 0,1,0 C. 1,0,0 D. 0,1,1 E. 1,1,0

347. For the state table below define the values of T_{A1} column.

A1	A0	T_{A1}	T_{A0}
0	0		1
0	1		1
1	0		0

A. 1,0,1 B. 0,1,0 C. 1,0,0 D. 0,1,1 E. 1,1,1

348. For the state table below define the values of T_{A0} column.

A1	A0	T_{A1}	T_{A0}
0	1	1	
1	0	0	
1	1	1	

A. 1,0,1 B. 0,1,0 C. 1,0,0 D. 0,1,1 E. 1,1,0

349. For the state table below define the values of T_{A1} column.

A1	A0	T_{A1}	T_{A0}
0	1		1
1	0		1
1	1		0

A. 1,0,1 B. 0,1,0 C. 1,0,0 D. 0,1,1 E. 1,1,1

350. For the state table below define the T_{A1} input function. T_{A1}= _____

A1	A0	T_{A1}	T_{A0}
0	0	0	1
0	1	1	1
1	0	1	0

A. $A_0 + A_1$ B. 1 C. 0 D. A_1 E. $A`_1$

351.For the state table below define the T_{A0} input function. T_{A0}= _____

Al	A0	T_{Al}	T_{A0}
0	0	0	1
0	1	1	1
1	0	1	0

A. A_0+A_1 B. 1 C. 0 D. A_1 E. $A`_1$

352. For the state table below define the T_{A1} input function. T_{A1}= _____

Al	A0	T_{Al}	T_{A0}
0	1	1	1
1	0	0	1
1	1	1	0

A. A_0+A_1 B. 1 C. 0 D. A_0 E. $A`_1$

353. For the state table below define the T_{A0} input function. T_{A0}= _____

Al	A0	T_{Al}	T_{A0}
0	1	1	1
1	0	0	1
1	1	1	0

A. $A`_0+A`_1$ B. 1 C. 0 D. A_1 E. $A`_1$

354. We have got function F (A,B,C). We want to implement it with multiplexer. If selection lines are A and B the table for expansion on C is:

A

	I_0	I_1	I_2	I_3
C`	0	1	2	3
C	4	5	6	7

B

	I_0	I_1	I_2	I_3
C`	0	1	4	5
C	2	3	6	7

C

	I_0	I_1	I_2	I_3
C`	0	2	4	6
C	1	3	5	7

D

	I_0	I_1	I_2	I_3
C`	0	1	2	6
C	3	4	5	7

E

	I_0	I_1	I_2	I_3
C`	0	1	3	6
C	2	4	5	7

355. We have got function F (A,B,C). We want to implement it with multiplexer. If selection lines are B and C the table for expansion on A is:

A

	I_0	I_1	I_2	I_3
A`	0	1	2	3
A	4	5	6	7

B

	I_0	I_1	I_2	I_3
A`	0	1	4	5
A	2	3	6	7

C

	I_0	I_1	I_2	I_3
A`	0	2	4	6
A	1	3	5	7

D

	I_0	I_1	I_2	I_3
A`	0	1	2	6
A	3	4	5	7

E

	I_0	I_1	I_2	I_3
A`	0	1	3	6
A	2	4	5	7

356. We have got function F (A,B,C). We want to implement it with multiplexer. If selection lines are A and C the table for expansion on B is:

A

	I_0	I_1	I_2	I_3
B`	0	1	2	3
B	4	5	6	7

B

	I_0	I_1	I_2	I_3
B`	0	1	4	5
B	2	3	6	7

C

	I_0	I_1	I_2	I_3
B`	0	2	4	6
B	1	3	5	7

D

	I_0	I_1	I_2	I_3
B`	0	1	2	6
B	3	4	5	7

E

	I_0	I_1	I_2	I_3
B`	0	1	3	6
B	2	4	5	7

357. Master-reset input is the input

A. to initialize the states of all flip-flops in the system
B. to initialize the states of all flip-flops in the system, when clock pulse will appear
C. to change the states of all flip-flops in the system
D. To clear all flip-flops asynchronously
E. to set all flip-flops asynchronously

358. For the circuit with the state table below we used D flip-flops. Then input equation for flip-flop A is ____.

A. $D_A = BX$ B. $D_A = AX+BX$ C. $D_A = BX'$ D. $D_A = BX+A$ E. $D_A = B'X$

Present state		Next state				Output	
		X=0		X=1		X=0	X=1
A	B	A	B	A	B	Y	Y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

359. For the circuit with the state table below we used D flip-flops. Then input equation for flip-flop B is ____.

A. $D_B = BX$ B. $D_B = AX+BX$ C. $D_B = BX'$ D. $D_B = BX+A$ E. $D_B = A'X$

Present state		Next state				Output	
		X=0		X=1		X=0	X=1
A	B	A	B	A	B	Y	Y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

360. For the circuit with the state table below we used D flip-flops. Then equation for output Y is ____.

A. $Y = BX$ B. $Y = AX+BX$ C. $Y = BX'$ D. $Y = BX'+AX'$ E. $Y = B'X$

Present state		Next state				Output	
		X=0		X=1		X=0	X=1
A	B	A	B	A	B	Y	Y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

361. For the circuit with the state table below we used D flip-flops. Then state equation for flip-flop A is ____.

A. $A(t+1) = BX$ B. $A(t+1) = AX+BX$ C. $A(t+1) = BX'$
D. $A(t+1) = BX+A$ E. $A(t+1) = B'X$

Present state		Next state				Output	
		X=0		X=1		X=0	X=1
A	B	A	B	A	B	Y	Y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

362. For the circuit with the state table below we used D flip-flops. Then state equation for flip-flop B is ____.

A. $B(t+1) = BX$ B. $B(t+1) = AX+BX$ C. $B(t+1) = BX'$
D. $B(t+1) = BX+A$ E. $B(t+1) = A'X$

Present state		Next state				Output	
		X=0		X=1		X=0	X=1
A	B	A	B	A	B	Y	Y
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

363. For the table below how many options to pass from state 0 to state 1? (X and Y are input variables).

A	X	Y	A(t+1)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

A. 1 B. 2 C. 3 D. 4 E. 5

364. For the table below how many options to pass from state 1 to state 0? (X and Y are input variables).

A	X	Y	A(t+1)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

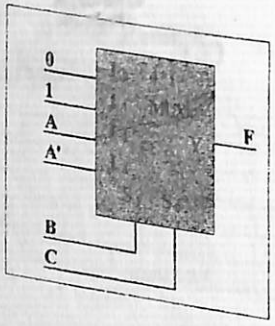
A. 1 B. 2 C.3 D. 4 E.5

365. For the table below what is input function for D flip=flop? (X and Y are input variables).

A	X	Y	A(t+1)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

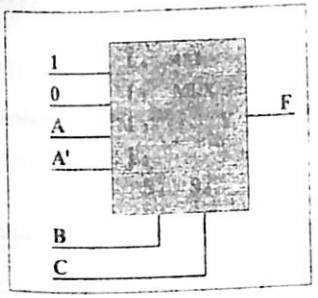
A. $D_A=AX`+X`Y+A`XY`$ B. $D_A= AX+BX$ C. $D_A= BX`$
D. $D_A= BX+A$ E. $D_A= B`X$

366. What function is implemented with multiplexer?



A. $F(A,B,C)=Ó(2,3,5,6)$
B. $F(A,B,C)=Ó(1,3,5,6)$
C. $F(A,B,C)=Ó(2,3,5,7)$
D. $F(A,B,C)=Ó(2,3,6,7)$
E. $F(A,B,C)=Ó(1,3,5,7)$

367. What function is implemented with multiplexer?



A. $F(A,B,C)=Ó(2,3,5,6)$
B. $F(A,B,C)=Ó(1,3,5,6)$
C. $F(A,B,C)=Ó(2,3,5,7)$
D. $F(A,B,C)=Ó(2,3,6,7)$
E. $F(A,B,C)=Ó(0,3,4,6)$

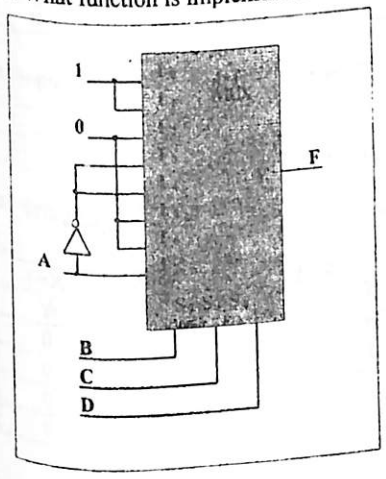
368. The two sequential circuits are said to be equivalent if

A. identical input sequences are applied to the two circuits
B. identical input sequences are applied to the two circuits and identical outputs occur for all input sequences
C. identical outputs occur for all input sequences
D. input and output sequences are equal
E. all above statements are wrong

369. Feedback shift register is such type of register, when

A. each flip-flop transfers its content to the next flip-flop
B. each flip-flop transfers its content to the next flip-flop, when a clock pulse occurs
C. each flip-flop transfers its content to the next flip-flop, when a clock pulse occurs, but the next state of the first flip-flop(for MSD) is some function of the present state of other flip-flops
D. each flip-flop transfers its content to the next flip-flop, when a clock pulse occurs, but the next state of the first flip-flop(for LSD) is some function of the present state of other flip-flops
E. each flip-flop transfers its content to the next flip-flop, when a clock pulse occurs, but the next state of the last flip-flop(for LSD) is some function of the present state of other flip-flops

370. What function is implemented with multiplexer?



A. $F(A,B,C,D)= Ó(0,1,3,5,7,14)$
B. $F(A,B,C,D)= Ó(0,1,3,4,7,14)$
C. $F(A,B,C,D)= Ó(0,1,3,4,8,15)$
D. $F(A,B,C,D)= Ó(0,1,3,4,8,9,15)$
E. $F(A,B,C,D)= Ó(0,1,3,5,7,14,15)$

371. To multiply $B_3B_2B_1B_0$ by $A_2A_1A_0$ it needs to use _____ 4-bit parallel full-adders.

A. 1 B. 2 C. 3 D. 4 E. 5

372. To multiply $B_2B_1B_0$ by $A_3A_2A_1A_0$ it needs to use _____ 4-bit parallel full-adders.

A. 1 B. 2 C. 3 D. 4 E. 5

373. For the circuit with the state table below we used D flip-flops. Show the sequence of next states of flip-flop A if D_A=AX+BX, if X=0.

A. 0,1,0,1 B.1,0,0,0 C. 0,1,1,1 D.0,0,0,0 E.0,1,1,0

Present state		Next state				Output	
		X=0		X=1		X=0	X=1
A	B	A	B	A	B	Y	Y
0	0		0	0	1	0	0
0	1		0	1	1	1	0
1	0		0	1	0	1	0
1	1		0	1	0	1	0

374. For the circuit with the state table below we used D flip-flops. Show the sequence of next states of flip-flop A if D_A=AX+BX, if X=1.

A. 0,1,0,1 B.1,0,0,0 C. 0,1,1,1 D.0,0,0,0 E.0,1,1,0

Present state		Next state				Output	
		X=0		X=1		X=0	X=1
A	B	A	B	A	B	Y	Y
0	0	0	0		1	0	0
0	1	0	0		1	1	0
1	0	0	0		0	1	0
1	1	0	0		0	1	0

375. For the circuit with the state table below we used D flip-flops. Show the sequence of next states of flip-flop B if D_B=A'X, if X=1.

A. 0,1,0,1 B.1,0,0,0 C. 0,1,1,1 D.0,0,0,0 E.1,1,0,0

Present state		Next state				Output	
		X=0		X=1		X=0	X=1
A	B	A	B	A	B	Y	Y
0	0	0	0	0		0	0
0	1	0	0	1		1	0
1	0	0	0	1		1	0
1	1	0	0	1		1	0

376. For the circuit with the state table below we used D flip-flops. Show the sequence of next states of flip-flop B if D_B=A'X, if X=0.

A. 0,1,0,1 B.1,0,0,0 C. 0,1,1,1 D.0,0,0,0 E.1,1,0,0

Present state		Next state				Output	
		X=0		X=1		X=0	X=1
A	B	A	B	A	B	Y	Y
0	0	0		0	1	0	0
0	1	0		1	1	1	0
1	0	0		1	0	1	0
1	1	0		1	0	1	0

377. For the circuit with the state table below we used D flip-flops. Show the sequence of outputs Y if output equation is Y=AX'+BX' and if X=0.

A. 0,1,0,1 B.1,0,0,0 C. 0,1,1,1 D.0,0,0,0 E.1,1,0,0

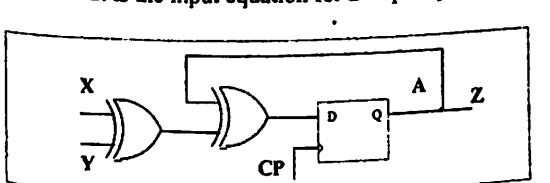
Present state		Next state				Output	
		X=0		X=1		X=0	X=1
A	B	A	B	A	B	Y	Y
0	0	0	0	0	1		0
0	1	0	0	1	1		0
1	0	0	0	1	0		0
1	1	0	0	1	0		0

378. For the circuit with the state table below we used D flip-flops. Show the sequence of outputs Y if output equation is Y=AX'+BX' and if X=1.

A. 0,1,0,1 B.1,0,0,0 C. 0,1,1,1 D.0,0,0,0 E.1,1,0,0

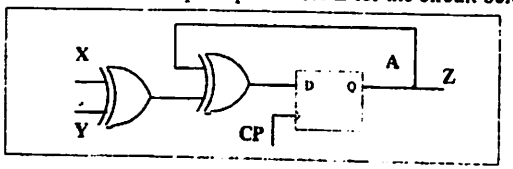
Present state		Next state				Output	
		X=0		X=1		X=0	X=1
A	B	A	B	A	B	Y	Y
0	0	0	0	0	1	0	
0	1	0	0	1	1	1	
1	0	0	0	1	0	1	
1	1	0	0	1	0	1	

379. What is the input equation for D flip-flop for the circuit below?



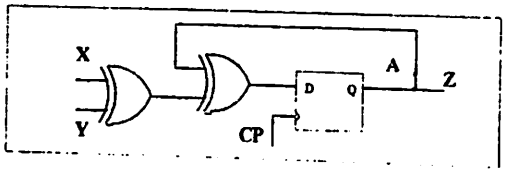
A. A+X
B. A⊕X
C. A⊕X⊕Y
D. X⊕Y
E. X⊕Y⊙A

380. What is the output equation for Z for the circuit below?



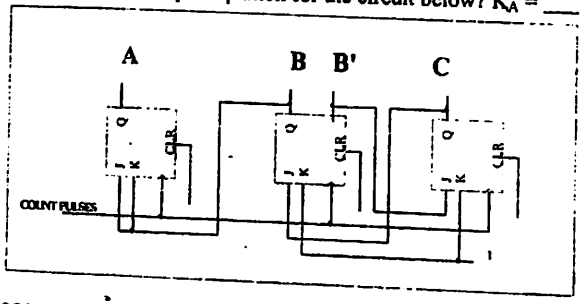
A. Z=A'
B. Z=A
C. Z=A⊕X⊕Y
D. Z=X⊕Y
E. Z=D(t+1)

381. What is the state equation for D flip-flop for the circuit below?



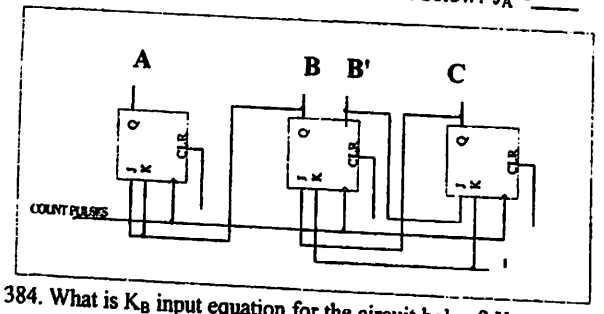
A. A+X
B. A⊕X
C. A⊕X⊕Y
D. X⊕Y
E. X⊕Y⊙A

382. What is K_A input equation for the circuit below? K_A =____



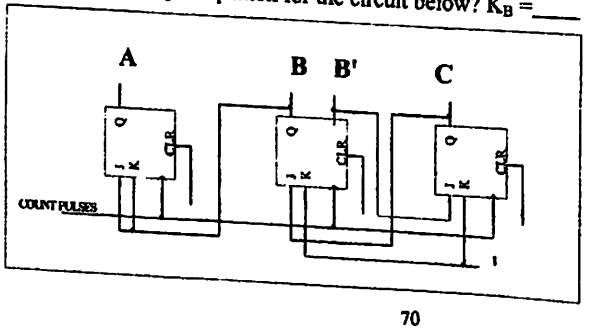
A. B'
B. B
C. A
D. A'
E. 1

383. What is J_A input equation for the circuit below? J_A =____



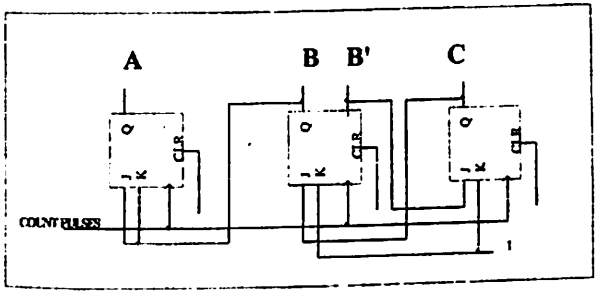
A. B'
B. B
C. A
D. A'
E. 1

384. What is K_B input equation for the circuit below? K_B =____



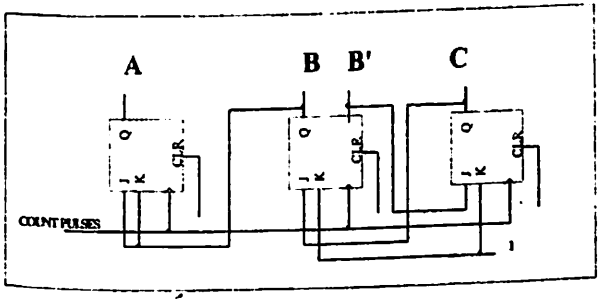
A. B'
B. B
C. A
D. A'
E. 1

385. What is J_B input equation for the circuit below? J_B =____



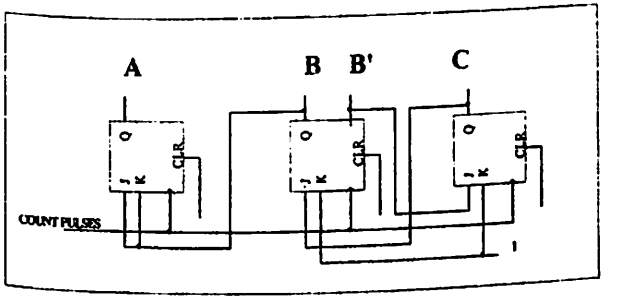
A. B'
B. B
C. C
D. A'
E. 1

386. What is K_C input equation for the circuit below? J_C =____



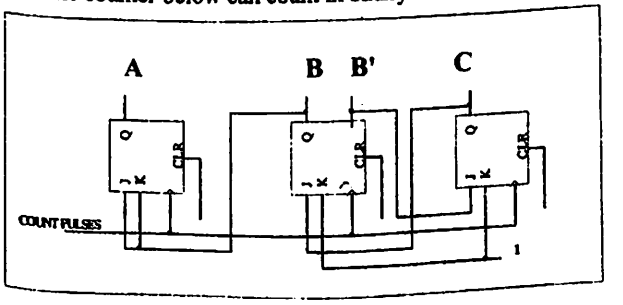
A. B'
B. B
C. A
D. A'
E. 1

387. What is J_C input equation for the circuit below? J_C =____



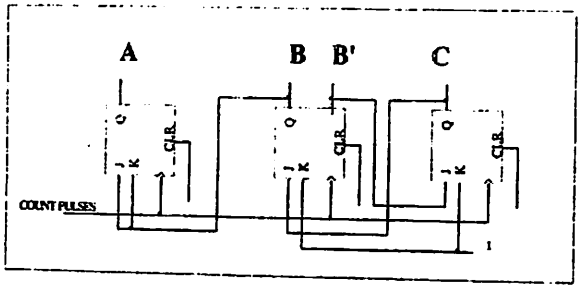
A. B'
B. B
C. A
D. A'
E. 1

388. The counter below can count in binary



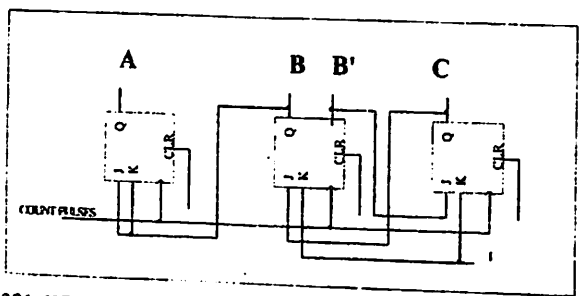
A. 0 to 9
B. 0,1,2,4,5,6
C. 0 to 15
D. 0 to 5
E. 0 to 7

389. What is the state of ABC for the circuit below after the third count pulse if the initial state was 010.



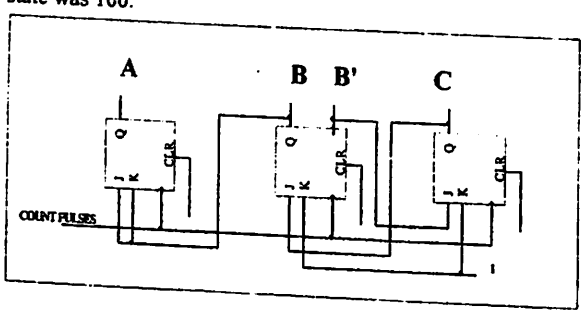
A.100
B. 101
C. 110
D. 111
E. 011

390. What is the state of ABC for the circuit below after the forth count pulse if the initial state was 001.



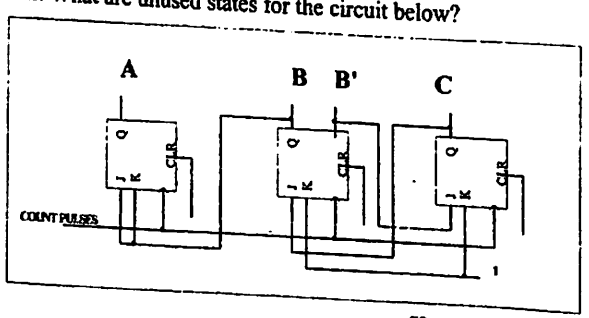
A.100
B. 101
C. 110
D. 111
E. 011

391. What is the state of ABC for the circuit below after the third count pulse if the initial state was 100.



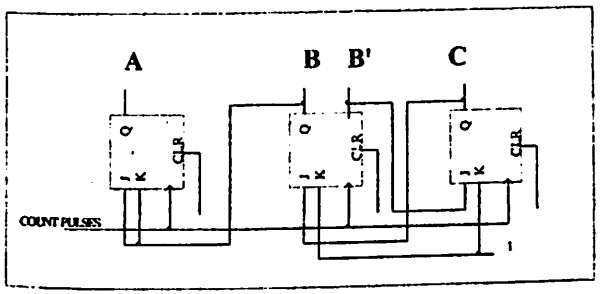
A.100
B. 101
C. 110
D. 111
E. 000

392. What are unused states for the circuit below?



A. 100,111
B. 011, 111
C. 000,111
D. 001, 110
E. 001,111

393. What states are used for the circuit below?



A. 000, 001, 010, 100, 101, 110
B. 000, 001, 010, 100, 101, 111
C. 000, 001, 010, 100, 110, 111
D 000, 001, 010, 101, 110, 111
E. 001, 010, 100, 101, 110, 111

394. For the table below the sequence for J_A is

A. X,X, X, 0,0,1 B. 0,0,1,X,X,X C. 0,1,X,0,1,X D. X,X,1,X,X,1 E. 1,1,0,1,0,0

Count sequence			Flip-flop inputs					
A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0		X	0	X	1	X
0	0	1		X	1	X	X	1
0	1	0		X	X	1	0	X
1	0	0		0	0	X	1	X
1	0	1		0	1	X	X	1
1	1	0		1	X	1	0	X

395. For the table below the sequence for K_A is

A. X,X, X, 0,0,1 B. 0,0,1,X,X,X C. 0,1,X,0,1,X D. X,X,1,X,X,1 E. 1,1,0,1,0,0

Count sequence			Flip-flop inputs					
A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0		0	X	1	X
0	0	1	0		1	X	X	1
0	1	0	1		X	1	0	X
1	0	0	X		0	X	1	X
1	0	1	X		1	X	X	1
1	1	0	X		X	1	0	X

396. For the table below the sequence for J_B is

A. X,X, X, 0,0,1 B. 0,0,1,X,X,X C. 0,1,X,0,1,X D. X,X,1,X,X,1 E. 1,1,0,1,0,0

Count sequence			Flip-flop inputs					
A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	X		X	1	X
0	0	1	0	X		X	X	1
0	1	0	1	X		1	0	X
1	0	0	X	0		X	1	X
1	0	1	X	0		X	X	1
1	1	0	X	1		1	0	X

397. For the table below the sequence for K_B is

A. X,X, X, 0,0,1 B. 0,0,1,X,X,X C. 0,1,X,0,1,X D. X,X,1,X,X,1 E. 1,1,0,1,0,0

Count sequence			Flip-flop inputs					
A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	X	0		1	X
0	0	1	0	X	1		X	1
0	1	0	1	X	X		0	X
1	0	0	X	0	0		1	X
1	0	1	X	0	1		X	1
1	1	0	X	1	X		0	X

398. For the table below the sequence for J_C is

A. 1,X,0,1,X,0 B. 0,0,1,X,X,X C. 0,1,X,0,1,X D. X,X,1,X,X,1 E. 1,1,0,1,0,0

Count sequence			Flip-flop inputs					
A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	X	0	X		X
0	0	1	0	X	1	X		1
0	1	0	1	X	X	1		X
1	0	0	X	0	0	X		X
1	0	1	X	0	1	X		1
1	1	0	X	1	X	1		X

399. For the table below the sequence for K_C is

A. X,X, X, 0,0,1 B. 0,0,1,X,X,X C. 0,1,X,0,1,X D. X,1,X,X,1,X E. 1,1,0,1,0,0

Count sequence			Flip-flop inputs					
A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	X	0	X	1	
0	0	1	0	X	1	X	X	
0	1	0	1	X	X	1	0	
1	0	0	X	0	0	X	1	
1	0	1	X	0	1	X	X	
1	1	0	X	1	X	1	0	

400. For the table below the sequence for J_C and K_C is

A. X,X, X, 0,0,1 0,0,1,X,X,X B. 0,1,X,0,1,X X,1,X,X,1,X
C. 1,1,0,1,0,0 X,X, X, 0,0,1 D. 0,0,1,X,X,X 0,1,X,0,1,X
E. 1,X,0,1X,0 X,1,X,X,1,X

Count sequence			Flip-flop inputs					
A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	X	0	X		
0	0	1	0	X	1	X		
0	1	0	1	X	X	1		
1	0	0	X	0	0	X		
1	0	1	X	0	1	X		
1	1	0	X	1	X	1		

401. For the table below the sequence for J_A and K_A is

A. X,X, X, 0,0,1 0,0,1,X,X,X B. 0,1,X,0,1,X X,1,X,X,1,X
C. 1,1,0,1,0,0 X,X, X, 0,0,1 D. 0,0,1,X,X,X X,X,X,0,0,1
E. 1,X,0,1X,0 X,1,X,X,1,X

Count sequence			Flip-flop inputs					
A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0			0	X	1	X
0	0	1			1	X	X	1
0	1	0			X	1	0	X
1	0	0			0	X	1	X
1	0	1			1	X	X	1
1	1	0			X	1	0	X

402. For the table below the sequence for J_B and K_B is

A. X,X, X, 0,0,1 0,0,1,X,X,X B. 0,1,X,0,1,X X,X,1,X,X,1
C. 1,1,0,1,0,0 X,X, X, 0,0,1 D. 0,0,1,X,X,X 0,1,X,0,1,X
E. 1,X,0,1X,0 X,1,X,X,1,X

Count sequence			Flip-flop inputs					
A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	X			1	X
0	0	1	0	X			X	1
0	1	0	1	X			0	X
1	0	0	X	0			1	X
1	0	1	X	0			X	1
1	1	0	X	1			0	X

403. For design of sequential circuit with JK flip-flop with state equation of A(t+1)=xAB+ yA'C+xy we must rearrange the equation and obtain such result:

A. J_A=yC+xy K_A=x'+y'B' B. J_A=yC+xy' K_A=x'+y'B' C. J_A=y'C+xy K_A=x'+y'B'
D. J_A=yC+xy K_A=x+y'B' E. J_A=yC+xy K_A=x'+yB'

404. For design of sequential circuit with JK flip-flop with state equation of A(t+1)=xAC+ y'BC we must rearrange the equation and obtain such result:

A. J_A=yC+xy K_A=x'+y'B' B. J_A=xAC K_A=x'+y'B' C. J_A=y'C+xy K_A=x'+y'B'
D. J_A=yC+xy K_A=x+y'B' E. J_A=xAC K_A=A'C+x'C+y'C

405. For design of sequential circuit with JK flip-flop with state equation of A(t+1)=x'B+ yAB' we must rearrange the equation and obtain such result:

A. J_A=yC+xy K_A=x'+y'B' B. J_A=yC+xy' K_A=x'+y'B' C. J_A=y'C+xy K_A=x'+y'B'
D. J_A=x'B+yAB' K_A=A'B+xB+y'B' E. J_A=yC+xy K_A=x'+yB'

406. Sequential MSI circuits may be

A. decoder, register, counter B. multiplexer, register, counter
C. demultiplexer , register, counter D. ROM, register, counter
E. register, counter, random-access memory

407. What statement is correct?

A. Number of different functions of two variables is equal to 8.
B. When the number of variables in a function is odd, the minterms with an even number of 0's are the same as the minterms with an odd number of 1's.
C. NOT is a binary operator
D. Tabulation method is not applicable for functions of 4 variables
E. Decoder with enable can be used as multiplexer

408. The transfer a new information into register is called _____ of register.

A. triggering B. Loading C. Set D. Reset E. none of above mentioned

409. Loading of register is done in parallel if

A. the bits of the register are loaded simultaneously
B. all the bits of the register are loaded simultaneously
C. all the bits of the register are loaded simultaneously with a clock pulse
D. all the bits of the register are loaded simultaneously with a single clock pulse
E. the bits of the register are loaded simultaneously with a single clock pulse

410. A digital system is said to operate in _____ when information is transferred and _____ one bit at a time. The content of one register is transferred to another by _____ the bits from one register to the other.

A. a serial mode ....manipulated .... loading
B. A parallel mode ..... manipulated ....shifting
C. a serial mode ....manipulated .... shifting
D. a serial mode ....shifted .... loading
E. a parallel mode ....shifted .... Loading

411. What statement is correct?

A. Number of different functions of two variables is equal to 8.
B. When the number of variables in a function is odd, the minterms with an even number of 0's are the same as the minterms with an odd number of 0's.
C. NOT is a binary operator
D. Computers may operate in a serial mode, a parallel mode, or in a combination of both.
E. Decoder with enable can be used as multiplexer

412. The time interval between clock pulses is called the _____, and the time required to shift the entire contents of a shift register is called the _____.

A. word time... bit time B. Bit time ... hold time C. Bit time ... word time
D. word time... setup time E. bit time.... hold time

413. In the _____ mode, information is available from all bits of a register and all bits can be transferred simultaneously _____. In the _____ mode, the registers have a single serial input and a single serial output. The information is transferred _____ while the registers are shifted in the same direction.

A. parallel....during one clock pulse ... serial... one bit at a time
B. parallel....during clock pulse... serial... one bit at a time
C. serial .... during one clock pulse ... parallel... one bit at a time
D. serial ... during clock pulse ... parallel... one bit at a time
E. parallel ...during the word time ... serial... one bit at a time

414. They are types of registers:

A. bidirectional shift register, unidirectional shift register
B. bidirectional shift register, unidirectional shift register, shift register with parallel load
C. bidirectional shift register, unidirectional shift register, register with parallel load
D. bidirectional register, unidirectional register, shift register with parallel load
E. bidirectional register, unidirectional register, register with parallel load

415. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the right, with the serial input being 101101. What is the content of the register after the first shift?

A. 0101 B. 1100 C. 1110 D. 1101 E. 1010

416. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the right, with the serial input being 101101. What is the content of the register after the second shift?

A. 0101 B. 1100 C. 1110 D. 1101 E. 0111

417. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the right, with the serial input being 101101. What is the content of the register after the third shift?

A. 0101 B. 1100 C. 1011 D. 1101 E. 1010

418. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the right, with the serial input being 101101. What is the content of the register after the forth shift?

A. 0101 B. 1100 C. 1110 D. 1101 E. 1010

419. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the right, with the serial input being 101101. What is the content of the register after the fifth shift?

A. 0110 B. 1100 C. 1110 D. 1101 E. 1010

420. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the right, with the serial input being 101101. What is the content of the register after the sixth shift?

A. 0101 B. 1100 C. 1110 D. 1011 E. 1010

421. How many flip-flops must be complemented in a 10-bit binary ripple counter to reach the next count after 0111111111?

A. 2 B. 4 C.6 D. 8 E. 10

422. How many flip-flops must be complemented in a 10-bit binary ripple counter to reach the next count after 0001010111?

A. 2 B. 4 C.6 D. 8 E. 10

423. How many flip-flops must be complemented in a 10-bit binary ripple counter to reach the next count after 0000101111?

A. 2 B. 4 C.5 D. 8 E. 10

424. A flip-flop has a 20-ns delay from the time its CP input goes from 1 to 0 to the time the output is complemented. What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops? What is the maximum frequency the counter can operate at reliably?

A. 5 MHz B. 6.25 MHz C. 8.33 MHz D. 10 MHz E. 12.25 MHz

425. A flip-flop has a 20-ns delay from the time its CP input goes from 1 to 0 to the time the output is complemented. What is the maximum delay in a 8-bit binary ripple counter that uses these flip-flops? What is the maximum frequency the counter can operate at reliably?

A. 5 MHz B. 6.25 MHz C. 8.33 MHz D. 10 MHz E. 12.25 MHz

426. A flip-flop has a 20-ns delay from the time its CP input goes from 1 to 0 to the time the output is complemented. What is the maximum delay in a 6-bit binary ripple counter that uses these flip-flops? What is the maximum frequency the counter can operate at reliably?

A. 5 MHz B. 6.25 MHz C. 8.33 MHz D. 10 MHz E. 12.25 MHz

427. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the left, with the serial input being 101101. What is the content of the register after the first shift?

A. 0101 B. 1100 C. 1110 D. 1101 E. 1011

428. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the left, with the serial input being 101101. What is the content of the register after the second shift?

A. 0110 B. 1100 C. 1110 D. 1101 E. 1010

429. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the left, with the serial input being 101101. What is the content of the register after the third shift?

A. 0101 B. 1100 C. 1110 D. 1101 E. 1010

430. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the left, with the serial input being 101101. What is the content of the register after the forth shift?

A. 0101 B. 1100 C. 1110 D. 1101 E. 1011

431. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the left, with the serial input being 101101. What is the content of the register after the fifth shift?

A. 0101 B. 1100 C. 0110 D. 1101 E. 1010

432. The content of a 4-bit shift register is initially 1101. The register is shifted 6 times to the left, with the serial input being 101101. What is the content of the register after the sixth shift?

A. 0101 B. 1100 C. 1110 D. 1101 E. 1010

433. What types of operation bidirectional shift register with parallel load has?

A. shift right, parallel load
B. shift left, parallel load
C. shift right, shift left, parallel load
D. Complement, no change
E. shift right, shift left, parallel load, no change

434. What statement is correct?

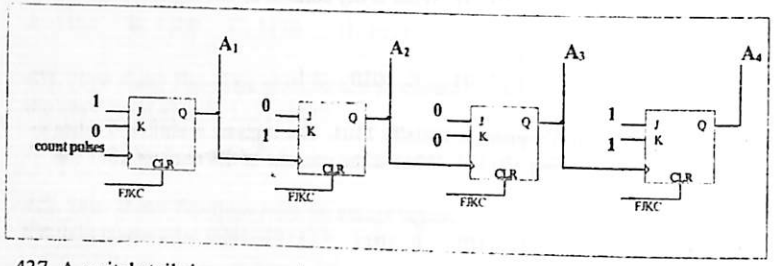
A. Number of different functions of two variables is equal to 8.
B. In a ripple counter, the flip-flop output transition serves as a source for triggering other flip-flops.
C. NOT is a binary operator
D. Computers may operate in a serial mode and in a parallel mode
E. Decoder with enable can be used as multiplexer

435. What statement is correct?

A. Number of different functions of two variables is equal to 8.
B. In a synchronous counter, the input pulses are applied to all CP inputs of all flip-flops.
C. NOT is a binary operator
D. Tabulation method is not applicable for functions of 4 variables
E. Decoder with enable can be used as multiplexer

436. What is the mistake in the circuit below?

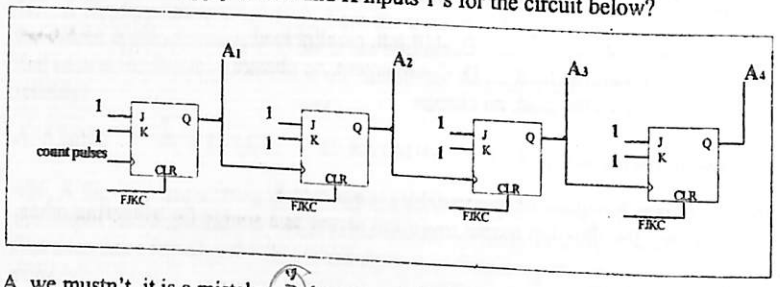
A. to all J inputs 0's must be applied B. to all J inputs 1's must be applied
C. to all K inputs 0's must be applied D. to all K inputs 1's must be applied
E. to all J and K inputs 1's must be applied



437. A switch-tail ring counter is

A. a register with a complement output of the last flip-flop connected to the input of the first flip-flop
B. a shift register with a complement output of the last flip-flop connected to the input of the first flip-flop
C. a circular shift register with a complement output of the last flip-flop connected to the input of the first flip-flop
D. a shift register with a complement output of the first flip-flop connected to the input of the last flip-flop
E. a circular shift register with a complement output of the first flip-flop connected to the input of the last flip-flop

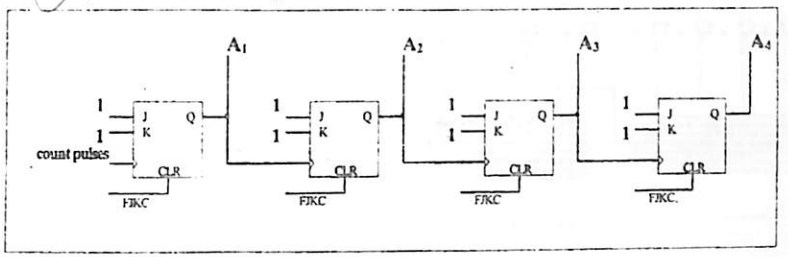
438. Why must we apply to all J and K inputs 1's for the circuit below?



A. we mustn't, it is a mistake B. because of JK flip-flop's property to change its state to complement one under action of such signals
C. because the aim is to obtain set state D. Because the aim is to obtain reset state
E. because the aim is to obtain 'no change" state

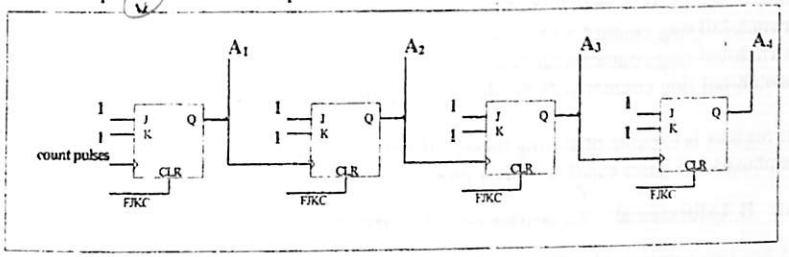
439. The circuit below can count _____.

A. up B. down C. up and down D. None E. It is not a counter



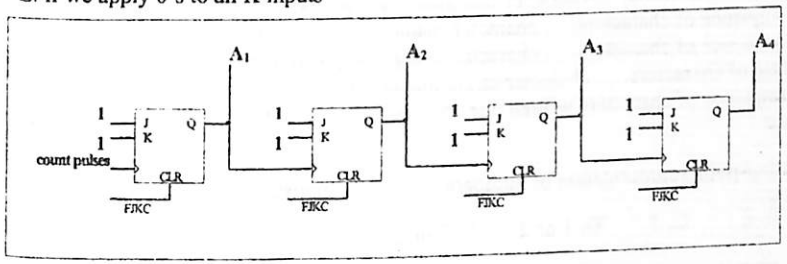
440. The circuit below can't count _____.

A. up B. down C. up and down D. None E. It is not a counter



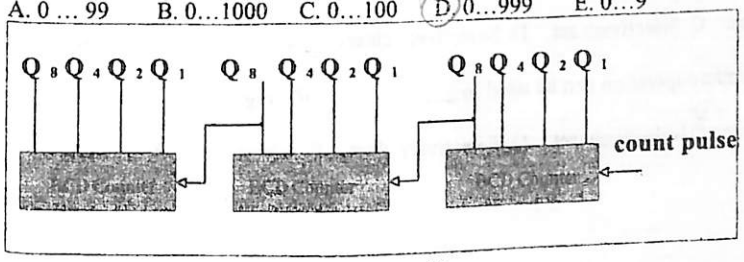
441. In what case the circuit below can count down?

A. if the outputs are taken from the complement terminals Q' of all flip-flops
B. if we apply 1's to all J inputs
C. if we apply 0's to all J inputs
D. if we apply 1's to all K inputs
E. if we apply 0's to all K inputs



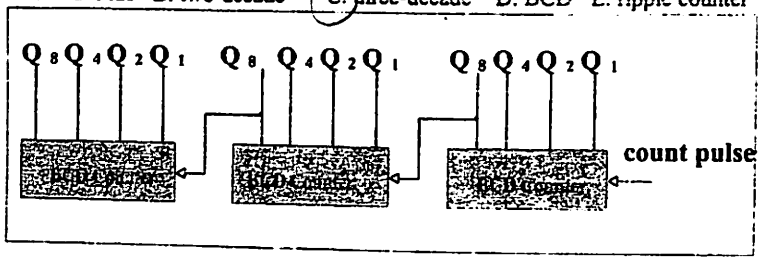
442. The circuit below can count from _____ to _____.

A. 0 ... 99 B. 0...1000 C. 0...100 D. 0...999 E. 0...9



443. The circuit below is_____ counter.

A. one-decade B. two-decade C. three-decade D. BCD E. ripple counter



444. Johnson counter is

A. a ring counter B. a switch-tail ring counter
C. a switch-tail ring counter with a decoder
D. a switch-tail ring counter with multiplexer
E. a switch-tail ring counter with the decoder requires only 2-input gates

445. If register is capable of storing binary information in its flip-flops and, in addition, has combinational gates capable of data-processing tasks, it is called _____ one.

A. shift B. bidirectional C. operational D. Memory E. unidirectional

446. When two numbers of n digits each are added and the sum occupies n+1 digits the phenomenon is called _____.

A. carry B. overflow C. floating-point data D. Nonnumeric data
E. none of above mentioned

447. A character string is _____. A computer can function as _____.

A. sequence of characters..... character-manipulating machine
B. finite sequence of characters..... character-manipulating machine
C. finite sequence of characters..... character-string manipulating machine
D. sequence of characters..... character-string manipulating machine
E. finite sequence of characters written one after another..... character-string-manipulating machine

448. Floating-point representation of numbers needs ____ registers.

A. 1 B. 2 C. 3 D. 1 or 2 E. 2 or 3

449. The XOR microoperation can be used to _____ bits of a register.

A. set B. clear C. selectively set D. Selectively clear E. selectively complement

450. The OR microoperation can be used to _____ bits of a register.

A. set B. clear C. selectively set D. Selectively clear E. selectively complement

451. The AND microoperation can be used to _____ bits of a register.

A. set B. clear C. selectively set D. Selectively clear E. selectively complement

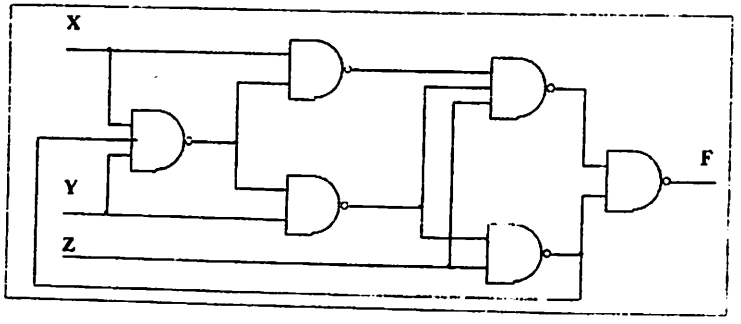
452. What statement is correct?

A. Number of different functions of two variables is equal to 8.
B. A statement that requires a sequence of microoperations for its implementation is called a macrooperation.
C. NOT is a binary operator
D. Computers may operate in a serial mode and in a parallel mode
E. Decoder with enable can be used as multiplexer

453. The operational code of an instruction is a group of bits that define an operation such as _____.

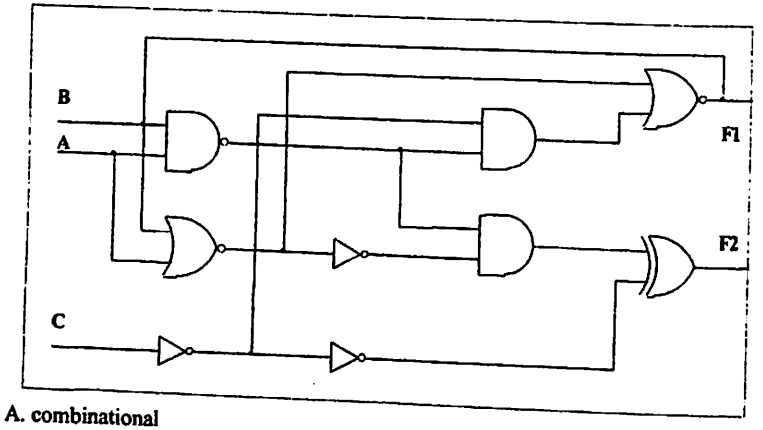
A) add, subtract, multiply, divide B. add, subtract, multiply, shift
C. add, subtract, multiply, complement D. add, subtract, divide, shift
E. add, subtract, multiply, shift, complement

454. The circuit below is



A. combinational B. sequential C. combinational, because it hasn't any flip-flops
D. sequential, because it has a feedback path
E. sequential, because it has a feedback path between output and input

455. The circuit below is



A. combinational
B. sequential
C. combinational, because it hasn't any flip-flops
D. sequential, because it has a feedback path
E. sequential, because it has a feedback path between output and input

CS 223 Digital Design

ANSWER KEY

1	A	46	B	91	C	136	C	181	D	226	A
2	E	47	A	92	C	137	E	182	D	227	D
3	A	48	D	93	D	138	A	183	A	228	C
4	A	49	C	94	B	139	B	184	B	229	E
5	E	50	B	95	E	140	E	185	C	230	C
6	C	51	B	96	D	141	C	186	A	231	C
7	B	52	B	97	A	142	D	187	B	232	B
8	D	53	A	98	C	143	E	188	C	233	E
9	A	54	E	99	E	144	C	189	D	234	E
10	A	55	B	100	B	145	C	190	A	235	D
11	E	56	D	101	A	146	B	191	B	236	B
12	B	57	B	102	E	147	E	192	C	237	D
13	A	58	D	103	B	148	B	193	D	238	E
14	E	59	E	104	E	149	E	194	C	239	A
15	C	60	B	105	D	150	D	195	B	240	A
16	A	61	A	106	D	151	D	196	D	241	B
17	E	62	E	107	D	152	C	197	D	242	C
18	C	63	D	108	C	153	E	198	E	243	E
19	B	64	C	109	C	154	E	199	C	244	C
20	D	65	E	110	B	155	C	200	D	245	E
21	E	66	C	111	A	156	D	201	E	246	D
22	D	67	B	112	C	157	A	202	B	247	E
23	C	68	C	113	A	158	B	203	D	248	C
24	A	69	A	114	E	159	C	204	B	249	D
25	A	70	D	115	A	160	B	205	C	250	C
26	C	71	E	116	A	161	D	206	C	251	A
27	D	72	B	117	D	162	A	207	D	252	A
28	B	73	D	118	B	163	C	208	E	253	B
29	C	74	D	119	A	164	C	209	D	254	B
30	B	75	E	120	E	165	E	210	A	255	C
31	D	76	E	121	E	166	A	211	B	256	C
32	E	77	C	122	D	167	E	212	E	257	A
33	C	78	C	123	E	168	C	213	C	258	E
34	A	79	C	124	A	169	B	214	B	259	C
35	A	80	A	125	E	170	A	215	D	260	C
36	D	81	E	126	C	171	B	216	C	261	E
37	E	82	C	127	D	172	D	217	C	262	B
38	C	83	C	128	D	173	A	218	B	263	C
39	B	84	D	129	D	174	B	219	B	264	D
40	E	85	B	130	A	175	D	220	B	265	E
41	B	86	B	131	E	176	C	221	B	266	E
42	D	87	C	132	A	177	C	222	A	267	B
43	E	88	A	133	E	178	C	223	D	268	A
44	A	89	B	134	E	179	B	224	C	269	D
45	D	90	E	135	A	180	A	225	E	270	E

271	E	316	B	361	B	406	E	451	D
272	E	317	A	362	E	407	B	452	B
273	B	318	B	363	B	408	B	453	E
274	D	319	B	364	B	409	D	454	E
275	E	320	E	365	A	410	C	455	E
276	B	321	D	366	B	411	D		
277	B	322	D	367	E	412	C		
278	B	323	A	368	B	413	A		
279	B	324	D	369	C	414	B		
280	D	325	C	370	D	415	C		
281	C	326	C	371	B	416	E		
282	E	327	D	372	C	417	C		
283	D	328	B	373	D	418	D		
284	B	329	B	374	C	419	A		
285	D	330	E	375	E	420	D		
286	D	331	B	376	D	421	E		
287	C	332	E	377	C	422	B		
288	B	333	A	378	D	423	C		
289	B	334	A	379	C	424	A		
290	A	335	C	380	B	425	B		
291	D	336	C	381	C	426	C		
292	A	337	A	382	B	427	E		
293	E	338	B	383	B	428	A		
294	B	339	E	384	E	429	D		
295	C	340	A	385	C	430	E		
296	D	341	B	386	E	431	C		
297	C	342	C	387	A	432	D		
298	B	343	E	388	B	433	E		
299	D	344	A	389	C	434	B		
300	A	345	B	390	C	435	B		
301	C	346	E	391	E	436	E		
302	E	347	D	392	B	437	C		
303	A	348	E	393	A	438	B		
304	D	349	A	394	B	439	A		
305	B	350	A	395	A	440	B		
306	E	351	E	396	C	441	A		
307	C	352	D	397	D	442	D		
308	E	353	A	398	A	443	C		
309	A	354	C	399	D	444	E		
310	E	355	A	400	E	445	C		
311	E	356	B	401	D	446	B		
312	E	357	A	402	B	447	E		
313	A	358	B	403	A	448	B		
314	E	359	E	404	E	449	E		
315	C	360	D	405	D	450	C		

Larissa A. Kiziyeva

DIGITAL DESIGN

Test questions

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ТОО «Эверо». Полиграфические услуги.
Тел.: 39-32-69, тел./факс: 32-38-43
e-mail: evero@nursat.kz